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Preface

This User's Manual is intended for novice users of the Logic Analyzer. Primary target user groups are:

- Secondary students in AB/AP, IB, or vocational programs.
- First year Applied Science students, second year Physical Science students, and above.
- Educators and academic researchers.
- Technicians and engineers with electronic or electrical backgrounds.

This User's Manual is designed and written for easy understanding. Users may expect ground knowledge and basic operational understanding from it, even without having the actual device or software nearby. A 10-minute glance at Chapter 4 should enable users to get started with Logic Analyzer. Though Logic Analyzer seems to be a simple plastic box, it can be used for advance academic research and industrial development. A detailed understanding of Chapter 4 is a necessity for progressing towards advanced developments and research applications.

This Manual has uniformed layouts for each chapter, and contents may have direct links to the index page. Every chapter consists of a **Front Page**, **Objective**, **Body Sections**, and **Conclusion**. The **Front Page** informs users the chapter number, title, exact # of sections contained, and the name of each instruction section. The **Objective** is meant to inform users exactly what will be learned. **Body Sections** consist of steps pertaining to a single task or function of Logic Analyzer. Contents in a **Body Section** are illustrations, in text or graph. A text illustration may be stepwise instructions or a paragraph not longer than nine lines. The **Conclusion** summarizes what has been demonstrated in a chapter and may be considered a quick review. An index page lists initial page number of chapters, as well as **Body Sections** (subsections in some chapters may be integrated into the index if they are fairly important). **Objectives** and **Conclusions** do not appear in the index.

Logic Analyzer is a highly sensitive electrical current sensing device. Users must carefully read instructions and procedures pertaining to installation and operation. Any instrument connected to Logic Analyzer should be properly grounded. A pair of anti-static gloves is strongly recommended when performing a task with Logic Analyzer. Furthermore, to ensure accuracy and consistency of output data, use the bundled components, or contact our service line for further assistance. User opinions are very important and to us. Contact us by telephone, fax, or email, if there is any further technical inquiry. Our engineering team will be very glad to assist you as soon as possible. Moreover, we also offer training for novice users with backgrounds in electronic related professions.

Finally, we sincerely thank you for choosing our product, and would like to hear back from you.

1 Features of the Zeroplus Logic Analyzer

- 1.1 Package Contents
- 1.2 Descriptions
- 1.3 Hardware Specifications
- 1.4 System Requirements
- 1.5 Safety Instructions and Advice

Objective

In this chapter, users will learn about the package contents, description, hardware specifications, system requirements, and safety issues of the Zeroplus Logic Analyzer. Though this chapter is purely informative, we highly recommend reading this carefully to ensure safety and accuracy when performing any operation with the Zeroplus Logic Analyzer.

1.1 Package Contents

When you first open the package, make sure you have the following components in the correct amounts. Otherwise, contact your retailer or our Customer Service department for further assistance.

Table 1-1: Parts list for retail packages

Models	LAP 16128U-A	LAP 32128U-A	LAP 321000U-A
Logic Analyzer	1	1	1
16-Pin Testing Cable	0	1	1
8-Pin Testing Cable	2	2	2
Probe	20	36	36
USB Cable	1	1	1
User's Manual*	1	1	1
Driver CD**	1	1	1
1-Pin Wire (White)	1	1	1
2-Pin Wire (Black)	1	1	1

* This is a hard copy of the User's Manual. The language may vary, depending on the region.

** This Driver CD consists of a multilingual software interface program, as well as a multilingual User's Manual.

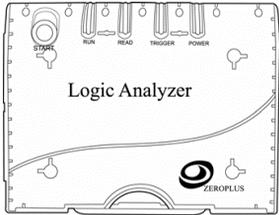
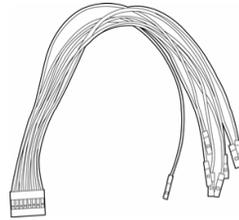


Fig. 1-1: Logic Analyzer



16-Pin x 1
8-Pin x 2

Fig. 1-2: Testing Cables

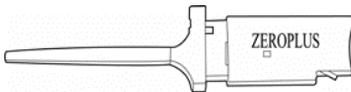


Fig. 1-3: Probes
(varied depending on models)



Fig. 1-4: USB Cable (1 set)



Fig. 1-5: User's Manual

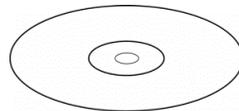


Fig. 1-6: Driver CD

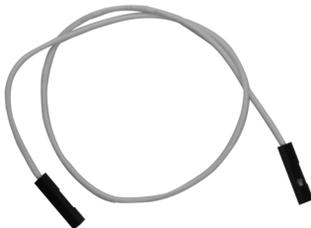


Fig. 1-7: 1-Pin External Clock Wire
(White)



Fig. 1-8: 2-Pin Ground Wire
(Black)

1.2 Descriptions

The appearances of the Zeroplus Logic Analyzer LAP-16128U-A, LAP-32128U-A, LAP-321000U-A all share the same features in the following figures. However, their internal chip sets are different.

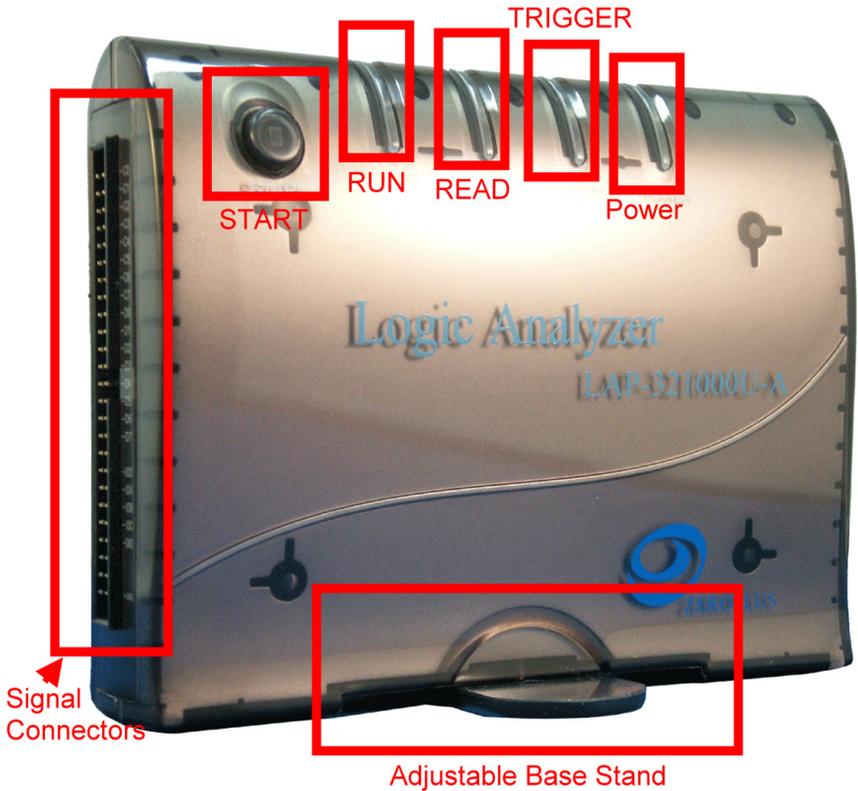


Fig. 1-9: A view of the Zeroplus Logic Analyzer LAP 321000U-A. see Fig 1-12, Table 1-2, Table 1-3, Table 1-4, and Table 1-5 for detailed information on the **Signal Connectors**.



Fig. 1-10: Side view of the ZeroPlus Logic Analyzer, which draws its power from the USB connection.

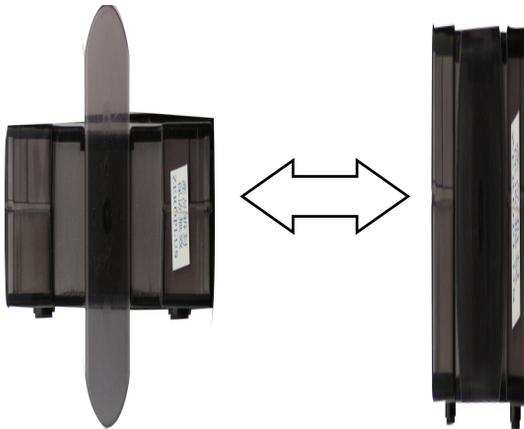


Fig. 1-11: The above graph illustrates how the Base Stand Support may be adjusted. Gently pull the plate apart from the ZeroPlus Logic Analyzer, rotate it 90° and release it.

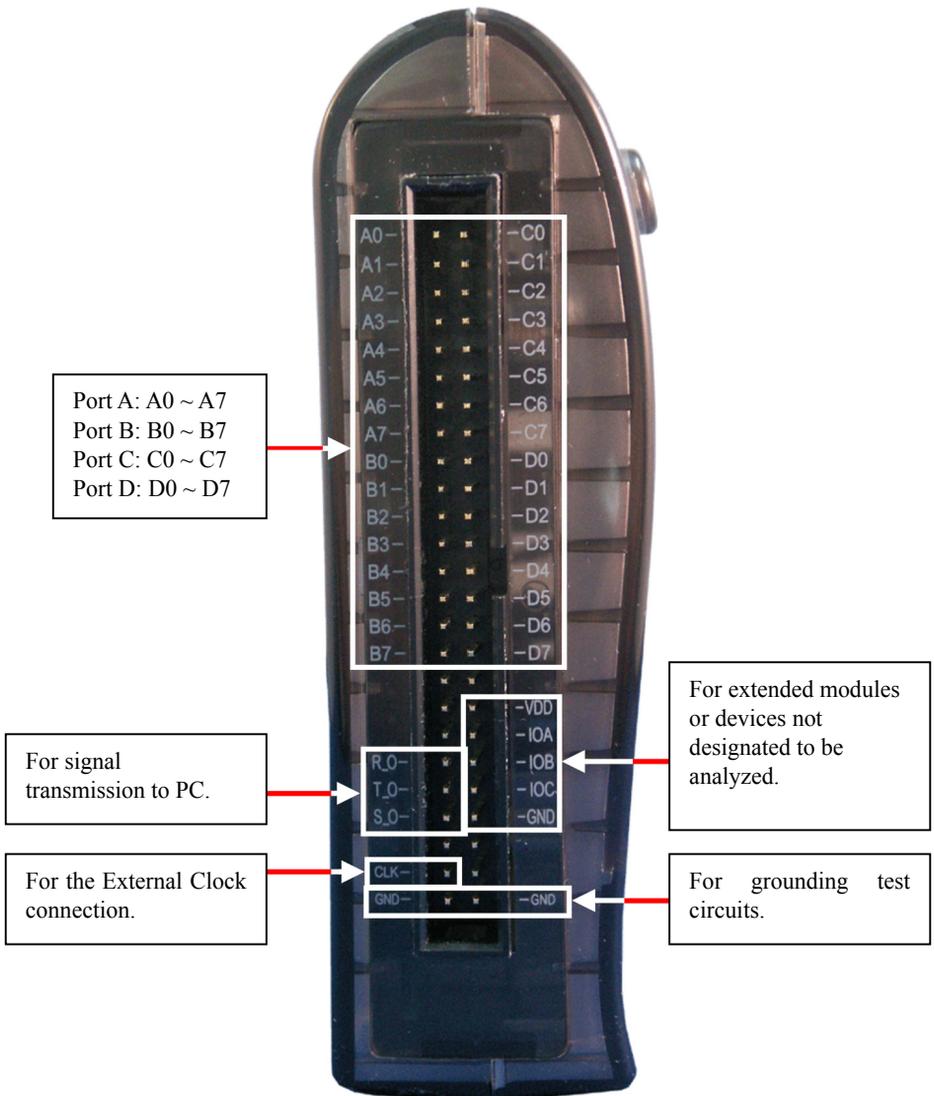


Fig. 1-12: Rear view of the ZeroPlus Logic Analyzer LAP 321000U-A. Rear views of LAP 16128U-A and 32128U-A might have minor differences. Read the next page for further information. Pins that do not have a sticker or labels printed beside them are not in use or connected to the ZeroPlus Logic Analyzer firmware.

Table 1-2: List of functional pins in each model.

Models	LAP 16128U-A	LAP 32128U-A	LAP 321000U-A
Port A (A0~A7)	√	√	√
Port B (B0~B7)	√	√	√
Port C (C0~B7)		√	√
Port D (D0~B7)		√	√
R_O			√
T_O			√
S_O			√
CLK	√	√	√
GND	√	√	√
VDD			√
IOA			√
IOB			√
IOC			√
GND			√

Table 1-3: Definitions and Functions of pins for all models.

CLK	Clock	Connects a given external module to be analyzed.
GND	Ground	Two pins used for grounding Logic Analyzer with a given external module to be analyzed.

Table 1-4: Definitions and Functions of pins for advanced models (1).

R_O	Read Out	When Logic Analyzer is about to upload data from memory to PC, the R_O will send a Rising Edge signal of DC3.3V. When upload is finished, a Falling Edge signal is sent to signal this fact.
T_O	Trigger Out	When a trigger condition is established, the T_O will send a Rising Edge signal of DC3.3V. When memory is full, a Falling Edge signal is sent to signal this fact.
S_O	Start Out	When a user initiates a sampling task by clicking the RUN icon in the window or clicking the START button on the device, the R_O will send a Rising Edge signal of DC3.3V. When Logic Analyzer finishes uploading, a falling edge signal is sent to signal this fact.

Table 1-5: Definitions and Functions of pins for advance models (2).

VDD	Voltage Drain (Semiconductor)	Provides +3.3 V for external modules by draining voltage from Logic Analyzer.
IOA	Ext. I/O Module A	Transmits signals from an external model or device not to be tested.
IOB	Ext. I/O Module B	Same as IOA .
IOC	Ext. I/O Module B	Same as IOA .
GND	Ground	Grounds external devices, in sequence

1.3 Hardware Specifications

Table 1-6: Hardware specifications of LAP-16128U-A and LAP-32xxxxU-A.

Items\Type	LAP-16128U	LAP-32128U-A	LAP-321000U-A
Interface	USB 2.0 (1.1)		
Operating System	Win 95/NT/98SE/ME/2000/XP/2003		
Power Supply	By USB 1.1 (Recommend USB 2.0)		
Channels	16	32	
Bandwidth	75MHz		
Memory	4M Bits		
Memory Depth (Per Channel)	256 Kbits	128 KBits	1.0 MBits
Internal Clock Rate (asynchronous)	100 Hz ~ 200 Mhz		
Max External Clock (synchronous)	Max 100MHz		
Trigger Channel	16 Channels	32 Channels	
Trigger Condition	Edge/Pattern		
Pre-Trigger/ Post-Trigger	Yes		
Trigger Level	1 Level		
Trigger Count	1-65535		
Max Trigger Page	Max 8191		
Enable Channel	16	32	
Enable	Pattern		
Enable Delay	Start: Edge and Pattern End: 1-65535		
Compression	16 Channel Compression	24 Channel Compression 1-255	

1.4 System Requirements

In this section, users obtain a rough idea of what operating system and hardware are required for Logic Analyzer. Depending on the preexisting PC configuration, Logic Analyzer software and hardware capabilities may vary. This manual assumes that users have clean installation of a mentioned operating system with a simple PC/workstation.

1.4.1 Operating System Requirements

In this subsection, we share our experiences testing the Zeroplus Logic Analyzer on the following Microsoft Windows operating systems. In order to activate the Zeroplus Logic Analyzer, an operating system must have driver software that supports USB.

Windows 95, 95 OS R2 (Compatibility with 95's is not so good since USB support especially USB 2.0 is not mature.)

- 1) Windows NT 4.0 Workstation & Server, Service Pack 6

(This is a very challenging operating system for Logic Analyzer. The trick is to mount the USB driver program, intended for DOS, at the beginning of the Windows NT startup process. This does not guarantee that Logic Analyzer will work, but it is worth trying)

- 2) Windows 98, 98 Second Edition, ME.

(We recommend Windows 98 SE; it has the best stability in the Win 9x series. Certainly, it works much better with Logic Analyzer than Windows NT.)

- 3) Windows 2000 Professional, Server Family

(32-Bit Version, Except **Data Center** version)

(We highly recommend Windows 2000 Professional, Server, or Advanced Server. Windows 2000's have very high compatibility and stability with Logic Analyzer. Windows 2000 takes almost any driver for any device. However, it does not have strong self-protection of its system kernel.)

- 4) Windows XP Home, Professional Editions (32-Bit versions)

(This is very interesting to work with. Though XP has very good PnP detection, it is not so driver friendly to devices without Microsoft certification. A considerable number of users find XP a little challenging, especially XP Service Pack 2. Logic Analyzer often appears to be **not properly installed**, but it works just fine with no problems.)

- 5) Windows Server 2003 Standard Edition, Enterprise Edition, Small Business Edition. (32-Bit Versions)

(Windows 2003 works much better than Windows XP, but a little worse than Windows 2000. The reason for this is unclear. We do not recommend using Logic Analyzer with Windows 2003 Datacenter Edition and Web Edition. Both are very difficult unless the user is an OEM builder.)

1.4.2 Hardware System Requirements

- **CPU**

For Windows NT, 95, 98, 98 SE, ME,
166 MHz, or above.

For Windows 2000, XP, 2003,
300 MHz, or above (strongly suggest 900 MHz, or above).

We have tested various 32-Bit and 64-Bit CPUs. Overall, we find that all 32-Bit CPUs work very well with Logic Analyzer software. Moreover, we find that AMD's 64-Bit CPUs, except Opteron, with a 64-Bit Windows operating system, work just fine with Logic Analyzer; no significant problems occur.

- **Memory**

For Windows NT, 95, 98, 98 SE, ME,
128 MB or above (64 MB is the minimum requirement).

For Windows 2000, XP, 2003,
256 MB or above (128 MB is the minimum requirement).

- **Hard Drive**

At least 100 MB free space.

- **USB**

USB 1.1 compatible or above (recommend USB 2.0).

- **Display Devices**

Recommend:

- 1 17" monitor with the resolution of 1024x786, or above.
- 2 8MB SDRAM on Video Card.

- **Power Supplies**

Since the Zeroplus Logic Analyzer requires power from a USB port, it is very important to have a very stable electric current supply. There are two major types of mechanisms used for retail power supplies: voltage transformers and voltage regulators. Voltage regulators mostly rely on an array of capacitors; the weight of this kind of power supply is very light. On the other hand, voltage transformers are hardware coiled and wired power supplies. Since voltage transformers consist of numerous metal parts, they may be double or heavier in weight than power supplies with voltage regulator technology, labeled with the same power. We recommend a power supply with hard wire-coiled voltage regulators.

1.5 Safety Instructions and Advice

The below information relates to storage and operation of Logic Analyzer. When using the Zeroplus Logic Analyzer, follow these instructions.

Table 1-7: General Advice

Cautions	Do not place heavy objects on the Zeroplus Logic Analyzer. Avoid hard impacts and rough handling. Logic Analyzer should avoid static electricity. Do not disassemble the Zeroplus Logic Analyzer; this could affect its operation and void the warranty.
Cleaning	Use a soft, damp cloth with a mild detergent to clean. Do not spray any liquid on the Zeroplus Logic Analyzer as it could enter the device. Do not use harsh chemicals or cleaners containing substances like benzene, toluene, xylene or acetone.

Table 1-8: Electrical Specifications

Items	Minimum	Typical	Maximum
Working Voltage	DC 4.5 V	DC 5.0 V	DC 5.5 V
Current at Rest			200 mA
Current at Work			400 mA
Power at Rest			1 W
Power at Work			2W
Error in Phase Off*			± 1.5 nS
V_{input} of Testing Channels			± DC 30 V
V_{Reference}	DC -6		DC +6 V
Input Resistance		500K Ω /10pF	
Working Temperature	5°C		70°C
Storage Temperature	-40°C		80°C

* refer to Section 8.2~8.4 for error analysis calculation.

Table 1-9: Operating Environment

WARNING	<p>Avoid direct sunlight Use in a dust free, non-conductive environment (see Note) Relative Humidity: < 80% Altitude: < 2000m Temperature: 0 ~ 40 degrees C</p> <p>This is a Class A product which may cause radio interference in a domestic environment.</p> <hr/> <p>Note: EN 61010-1:2001 specify degrees of pollution and their requirements. Logic Analyzer falls under Level 2.</p> <p>Pollution refers to 'addition of foreign matter, solid, liquid or gaseous (ionized gases), that may produce a reduction of dielectric strength or surface resistivity'.</p> <p>Pollution Degree 1: No pollution or only dry, non-conductive pollution occurs. This pollution has no effect.</p> <p>Pollution Degree 2: Normally only non-conductive pollution occurs. Occasionally, however, temporary conductivity caused by condensation must be expected.</p> <p>Pollution Degree 3: Conductive pollution occurs or dry, non-conductive pollution occurs which becomes conductive due to condensation, which is expected. In such conditions, equipment is normally protected against exposure to direct sunlight, precipitation and wind, but neither temperature nor humidity is controlled.</p>
Storage Environment	<p>Location: Indoors Relative Humidity: < 80% Temperature: 0 ~ 50 Degrees C</p>

Conclusion

After reading this chapter, users should have a basic grasp of Logic Analyzer. A complete understanding of the **Safety Instructions and Advice** is the critical prerequisite of any further operation, which is demonstrated in subsequent chapters.

2 Installations

- 2.1 Software Installation
- 2.2 Hardware Installation
- 2.3 Tips and Advice

Objective

In this chapter, there are only two objectives to be accomplished: software installation, and hardware installation. Most hardware installation step may be substituted by referring to Section 1.2. Steps pertaining to software installation must be followed step by step to ensure successful installation, for the hardware drive is rapped into the installation program and can no be separate by any conventional methods.

2.1 Software Installation

In this section, users will learn how to install the software interface and the hardware driver software. Just like install any other USB device, Application software and driver software must be installed prior to the hardware connection. Here is a demonstration of installing Logic Analyzer **LAP-32128U-A**. The other two models mentions in Chapter 1 have identical procedures like **LAP-32128U-A**. Users many follow the same procedures.

Step 1. Place the driver CD from the retail package on the tray of a CD-ROM (or other compatible optical devices which must have trays).

Step 2. Execute the installation program. There are two ways to do this.

Method 1: Go to the START menu, click START → Run, and then enter the following path and command name. See Fig. 2-1.

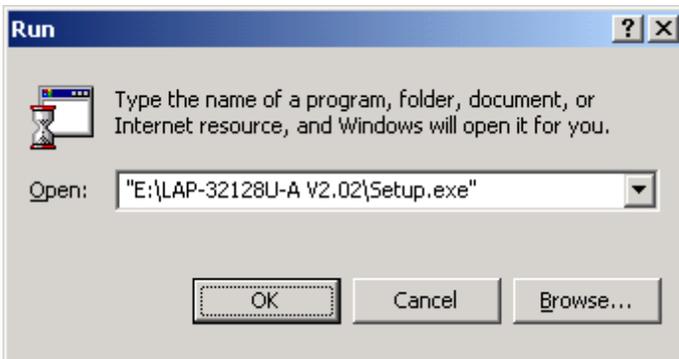


Fig. 2-1: The complete installation command. The double quotation marks are optional. In this case, "E" is the label of my CD-ROM Drive.

Method 2: Go to the My Computer, and then follow the graphic illustrations below.

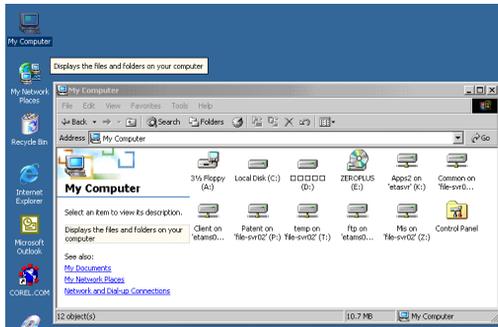


Fig. 2-2 – My Computer

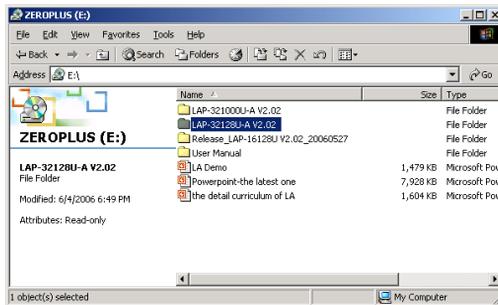


Fig. 2-3 – CD Rom Menu Structure

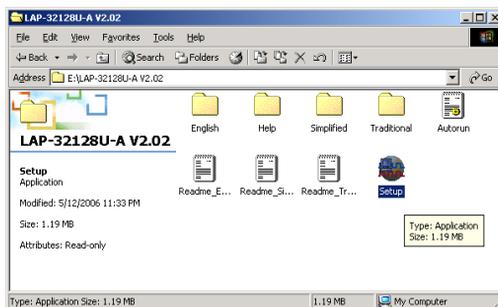


Fig. 2-4: Click the **Setup.exe** icon. The installation will proceed. We highly recommend terminating all other programs before setup.



Fig. 2-5: The Install Program. Choose the language you desire.
For demonstration purposes, we choose English.



Fig. 2-6: The program should proceed if there are no other errors.

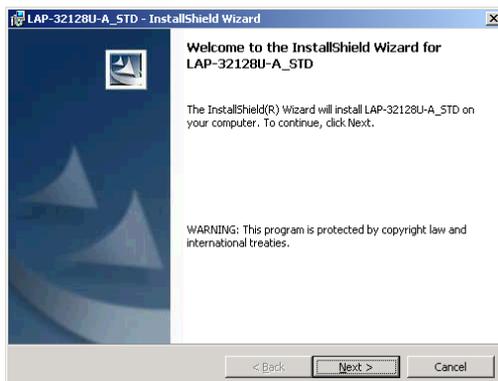


Fig. 2-7: Click **Next** to proceed.



Fig. 2-8: Select “I accept the term in this license agreement, ” and click **Next**.

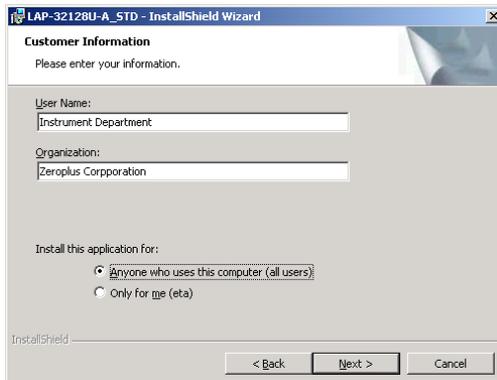


Fig. 2-9: Enter your name and organization information.
You may also choose how you are going to share this program with others or not.



Fig. 2-10: Choose the setup type. We recommend **Complete** for novice.



Fig. 2-11: This is the configuration page for Custom Setup.

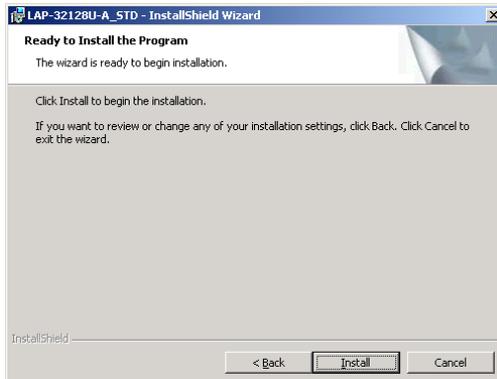


Fig. 2-12: This is just for confirmation that you want to install the program.

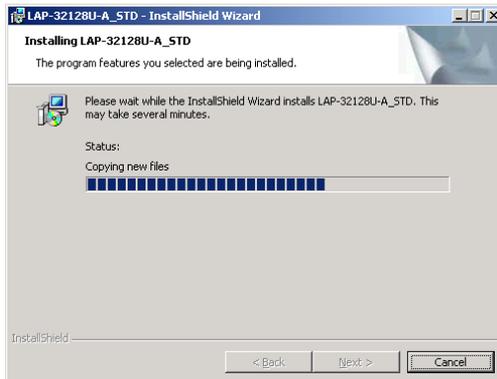


Fig. 2-13: The installation in progress.



Fig. 2-14: The system will ask you to confirm the installation of the USB device program for Logic Analyzer to Windows. Press **Yes** to proceed.

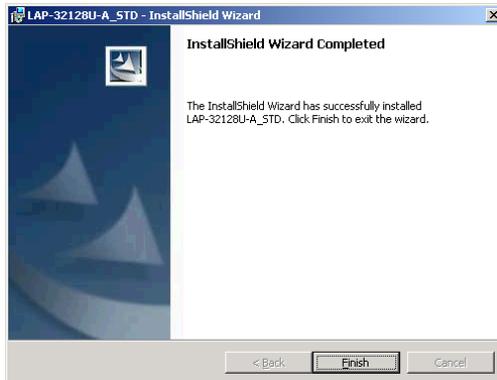


Fig. 2-15: Installation completed.



Fig. 2-16: Restart in order to refresh your system settings.

2.2 Hardware Installation

Hardware installation will be relatively much easier than the software installation, for the only thing to do is to connect Logic Analyzer to your computer with a USB Cable. There are a few steps to be followed.

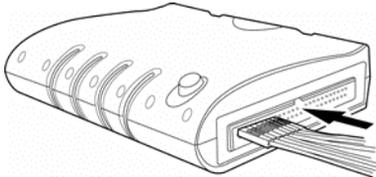


Fig. 2-17

1. Plug the fixed end of the cables into the LA(Fig.2-17).

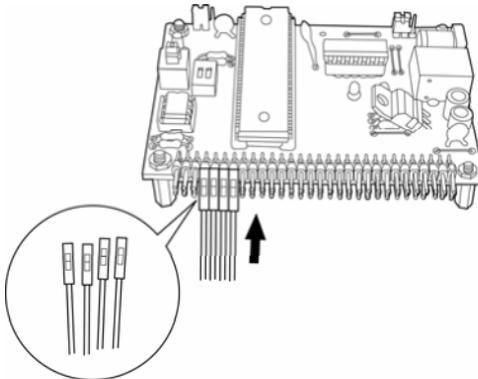


Fig. 2-18

2. Plug the loose ends into the connectors on the circuit board to be analyzed(Fig.2-18).

Note: The following sequence must be observed when connecting the connectors into the circuit board: A0 = Brown, A2 = Red, A3=Orange and so on.

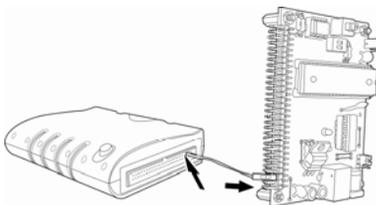


Fig. 2-19

3. The circuit board must be grounded to the LA with the connecting cables(Fig.2-19).

- Step 1 - Plug the thin male end of the USB cable into the laptop or PC.
- Step 2 - Plug the square female end into the logic analyzer.

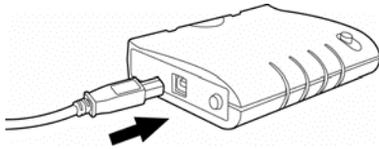


Fig. 2-20

4. Plug the square end of the USB cable into the Logic Analyzer(Fig.2-20).

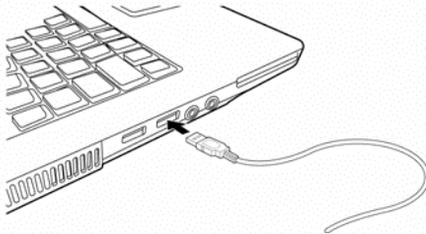


Fig. 2-21

5. Plug the thin end into the computer(Fig.2-21).

At this point, the computer should be able to detect the Logic Analyzer and finalize the installation for hardware connection. Refer to Chapter 5 for Troubleshooting and Chapter 6 for FAQ. Otherwise, contact our Service Department for any assistance via telephone, fax, or email.

Here we like to show how things look after assembling.

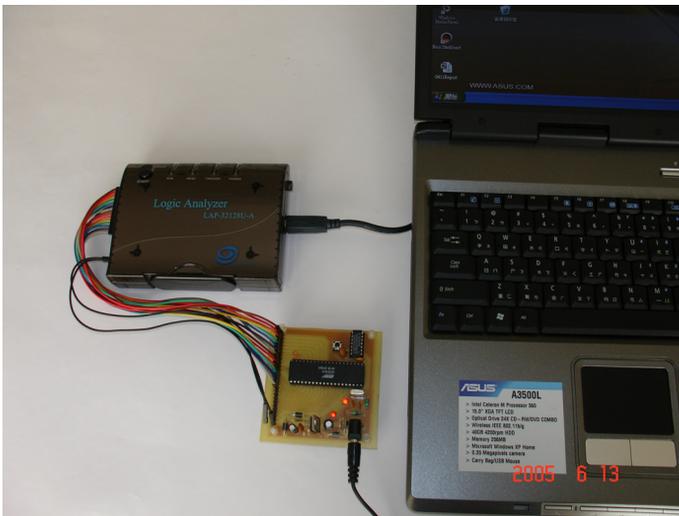


Fig. 2-22: An assembly of Laptop, Logic Analyzer, and a testing board.

2.3 Tips and Advice

1. When testing a circuit board, make sure that the internal sampling frequency (within the Logic Analyzer) is at least four times the external board frequency.
2. We highly recommend Microsoft Windows 2000 with a USB 2.0 port; this system is very simple and stable, and USB 2.0 gives much better power and data supply.
3. If the signal connector does not work well with the pins on the test board, try using the supplied probes.

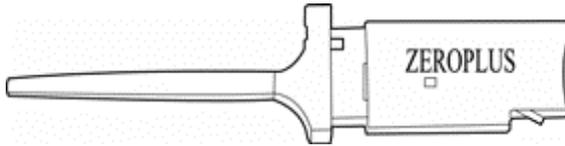


Fig. 2-23: Probes comewith the retail package.

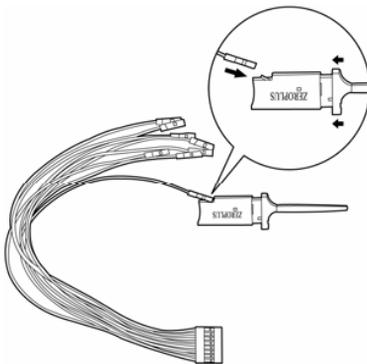


Fig. 2-24

- 3-1. Take the loose end of the cable and insert it into the clip as shown opposite (Fig.2-24).

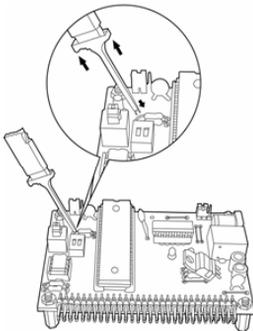


Fig. 2-25

- 3-2. Using the thumb on the back of the end of the clip and the first 2 fingers of the hand push the plastic cover back to reveal 2 metal prongs (Fig.2-25).
- 3-3. Place the metal prongs on a metal connector on the motherboard and release the fingers so that the prongs grip the metal connector (Fig.2-25).

4. Always have your Internet connection on; software updates may arrive anytime. The Logic Analyzer software will connect to the server for updates.
5. If there are unwanted signals and there is guidance for what is needs to be filtrated out, use Enable or the Enable Delay function.
6. When measuring for a long period, Compression makes memory more efficient.
7. Trigger condition depends on the test board. If triggering does not work well, try narrowing the trigger conditions and optimize them repeatedly.
8. If a test board has a lower frequency than Logic Analyzer, sample signals according to the external clock.
9. When clocking by an external clock, filter extra signals with the Enable function.
10. When analyzing a signal that seems to have an unknown signal pattern, make a circuit signal decoder to duplicate signals in the same pattern. Afterwards, connect the alternative circuit to Logic Analyzer for further analysis of said pattern.
11. You may wish to remove channels that Logic Analyzer is not currently connected to from the Bus/Signal display. Bus/Signal (Menu) → Channel Setup. You can then delete unnecessary channels.

Conclusion

Installation steps should be fairly easy followed. When connecting to a designated testing circuit board, we strongly recommend you referring to Chapter 1 Fig. 1-12, Table 1-2, Table 1-3, Table 1-4, Table 1-8, and Table 1-9 for detail information and safety notes.

3 User Interface

- 3.1 Menu Bar & Tool Bar
- 3.2 Find Data Value
- 3.3 Statistics Feature
- 3.4 Customize Interface

Objective

Chapter 3 presents detailed information on the Logic Analyzer software interface in four sections: **Menu Bar**, **Tool Bar**, **Statistical Function**, and **Interface Customization**.

Basic Layout

The layout of the Logic Analyzer software interface can be divided into eight sections shown in the following figure.

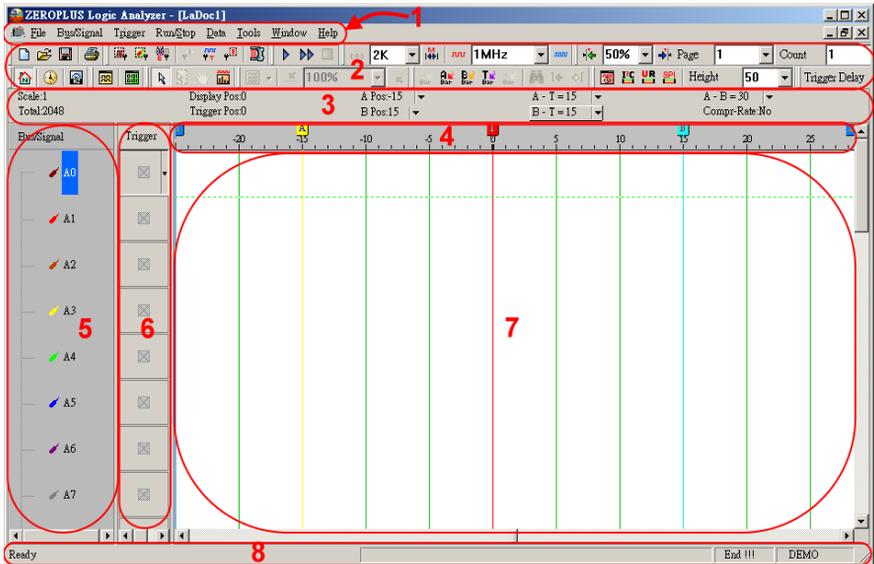


Fig 3-1 – Software Interface

1. Menu Bar

You can perform all operations directly from this Menu, including configure label, rename, execute and stop. Pull-down menus let you quickly and easily navigate through your measurement to get the view you want.

2. Toolbar

The Toolbar is the graphical user interface which enables you to work with some of the more common applications. From these icons, you can change settings and operate the Logic Analyzer easily.

3. Information Bar

Displays information about the grids in the waveform, for example: Address, Time, Frequency, Trigger Bar, A Bar, B Bar and other Bar. Details of the labels are below:

Scale -	Defines the acquisition clock that controls the data sampling
Total -	The period of time that Logic Analyzer capture data.
Display Pos -	The middle tip means the middle position of waveform.
Trigger Pos -	Trigger position.
A Pos -	The main function is setting A Bar or the other Bar.
B Pos -	The main function is setting B Bar or the other Bar.
A-B -	Press the under arrow to exchange and become the other Bar moreover, you also execute this function form the other Bar.

4. Ruler (in wave form display / in listing Display)

Ruler shows the time position of wave show in wave display area.

5. Bus/Signal (in wave Form Display / in listing display)

The name of the measured channel: it is much clearer to understand the object connecting with the one of measured channels moreover it also matches the color to show. Furthermore, help you know the color of the connecting line ,it is easy to look for the signal and to lower the wrong rate of the signal.

6. Trigger Column

Trigger Column allow users to adjust signal trigger conditions.

7. Display area

This area is where you can view the acquired data as a waveform or in a listing format.

Waveform Display

This interface shows the digital signals directly. When the signal is on "0", the waveform will be displayed as  . 

If signal is on "1", the waveform is as  , an unknown signal waveform is displayed as gray color for the middle line between the high and low levels as  . In waveform format, the continue signal will be constructed as below. There are sixteen channels in LAP-16128U, and thirty two channels in LAP-32128U-A.

Listing Display

This interface shows the digital signals as 1's and 0's. The high level is displayed as "1" and low level is displayed as "0".

8. Status area

You can get the status of the Logic analyzer system processed. The function name is also indicated here.

3.1 Menu Bar & Tool Bar

Section 3.1 presents detailed information on the eight menu items shown in the menu bar and twelve Tool item. These eight menu items are **File**, **Bus/Signal**, **Trigger**, **Run/Stop**, **Data**, **Tools**, **Window**, and **Help**. These twelve tool items are **Standard**, **Trigger**, **Run/Stop**, **Sampling**, **Trigger Content Set**, **Display Mode**, **Window**, **Mouse Pattern**, **Zoom**, **Data**, **Show Time/Height**, and **Trigger Delay**.

File

 New	Ctrl+N	
 Open...	Ctrl+O	
Close	Ctrl+F4	← Close - closes the file being worked on.
 Save	Ctrl+S	
Save As...		
Export...	Ctrl+Shift+E	← Export workspace into Text (*.txt) and CSV Files (*.csv)
Capture Window...	Ctrl+C	
Language		← Language allows users to change the language interface of menus, tool boxes, etc.
 Print...	Ctrl+P	
Print Preview		← Print Preview shows three options: Bus/Signal, Trigger option, and Position Display Area (See Fig. on Page).
Print Setup...		
Recent File		
Exit		← Exit the program.

Fig 3-2: **File** menu.



Fig 3-3: **Standard** tool bar.

Menu Bar: File

Menu Item	Menu & Dialogue Window
 New Ctrl+N	Open a New file.

 **Open...** Ctrl+O

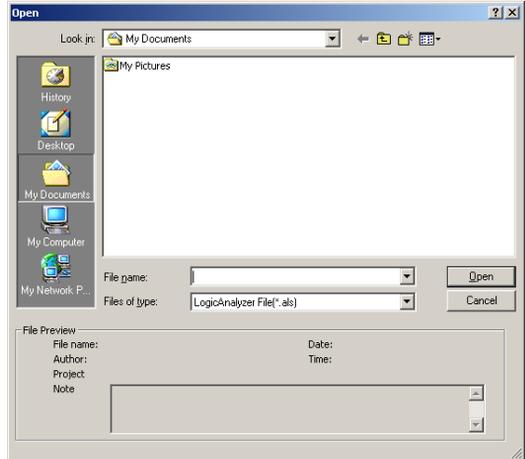


Fig 3-4: Open an existing file.

Close Ctrl+F4

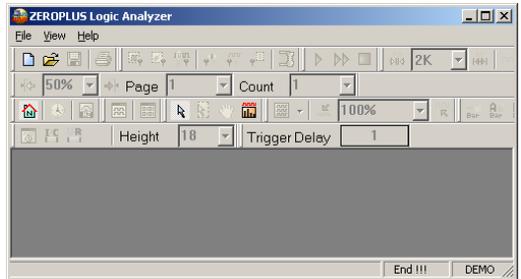


Fig 3-5: Close the active workspace.

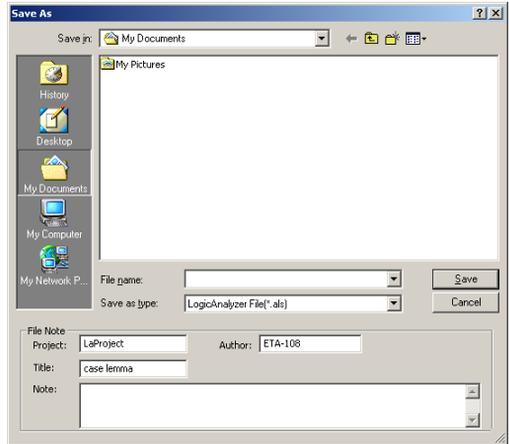


Fig 3-6 – Save As window

Save – Saves the current file.

Save As – Specify the name of the file to be saved.

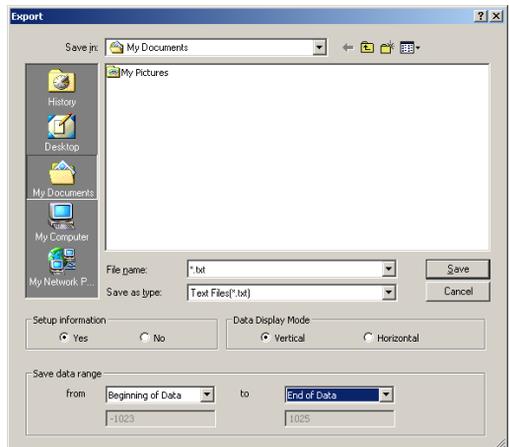


Fig 3-7 – Export Window

Export a file into text (*.txt) or CSV (*.csv) formats.

Display Parameter: Decide whether or not to display the parameters of the file to be exported.

Data Display Mode: Choose whether to export the data either vertically or horizontally.

Display Data's Range: Choose the range of the data to export from the drop down menus.

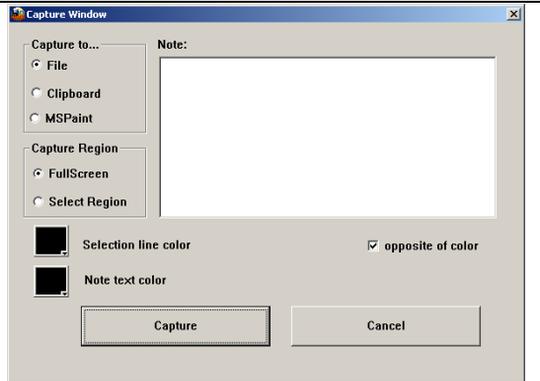


Fig 3-8: **Capture Window**

This feature is equivalent to [Alt]+[Print Screen], or [Print Screen]

Capture to

- File – saves the capture image as either a jpeg or bmp
- Clipboard – Copies the captured image to the clipboard for use in other applications.
- MsPaint – Directly starts MSPaint to view the captured image.

Capture Window... Ctrl+C

Capture Range

- Full Screen – capture everything on the screen.
- Select Region – after pressing the capture button a cross-hair will appear on the screen. Left click the mouse button to drag an area to capture.

Selection Line Color – click the color box to change the color

Opposite of color – Click this check box to ensure that the note text will be the opposite of the line color.

Color of the note – Choose the color of note text.

Note – Type in a note to attach to the captured image.

Capture Button – Click the capture button to capture the image

Cancel - Click cancel to end the capture.

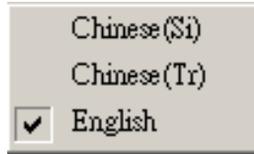


Fig 3-9: Choose between Chinese Simplified (si), Chinese Traditional (Tr) and English.

Language



Fig 3-10: When changing languages the following screen will be displayed and the program will need to be restarted.

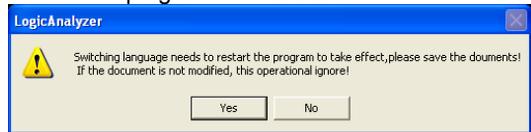


Fig. 3-11: Press Yes to close all open applications and restart the system.

Print... Ctrl+P

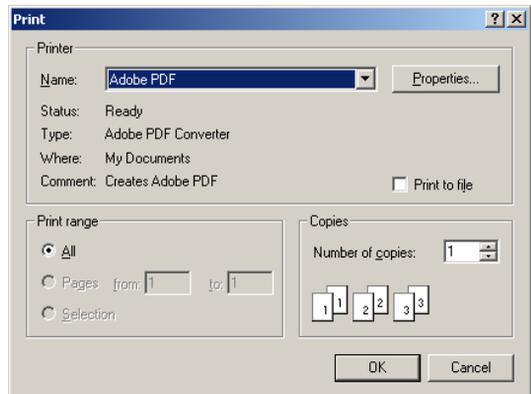


Fig 3-12: Click to enter the **Printer** dialogue box.

Print Preview

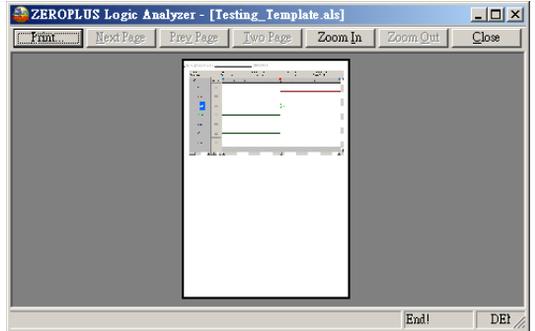


Fig 3-13 Click to show a **Preview** of the **Print**.

Print Setup...



Fig 3-14: Click to enter the Print Setup
dialogue window.

Recent File

Shows recently saved file.

Exit

Exit the program.

Bus/Signal

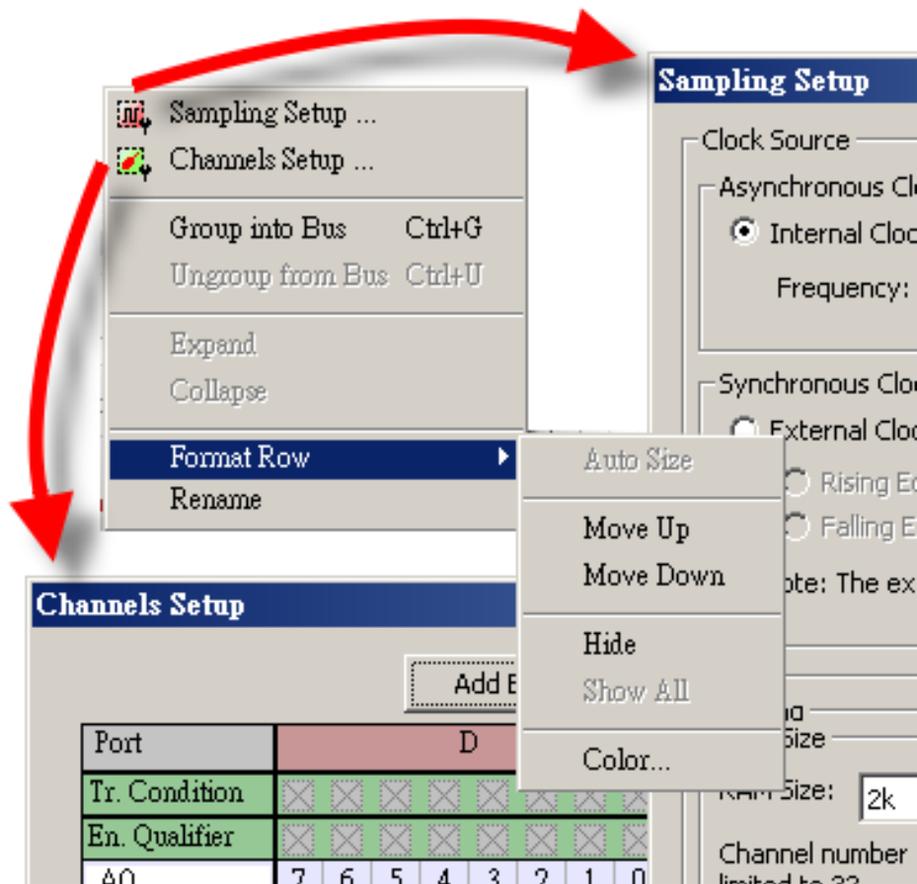


Fig 3-15: **Bus/Signal** menu. Dialogue windows of the Sampling Setup and Channel Setup are shown and indicated by arrows.



Fig 3-16: **Trigger** tool box.

Menu Bar: **Bus/Signal**

Menu Item

Detail Menu or Dialogue Window

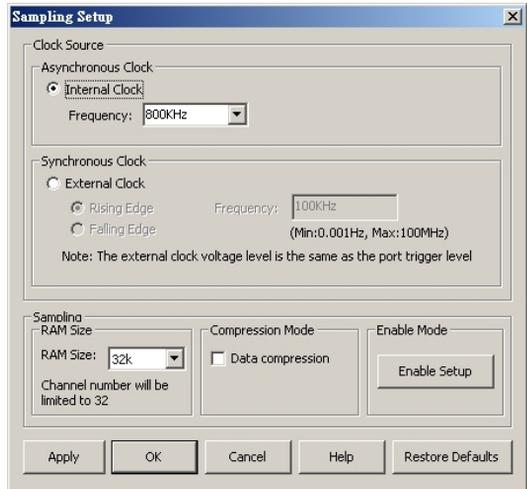
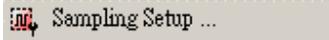


Fig 3-17: Sampling Setup

Tip:

See section 4.1 for detailed instructions.

Icon	Description
	Decrease RAM size
	Increase RAM size
	Decrease internal clock frequency
	Increase internal clock frequency



Fig-3-18 – RAM Size

Choose the RAM size and the internal clock frequency from the drop down menus.

Ram Size

The amount of acquired data that can be stored by the logic analyzer depends on the amount of allocated RAM.

The total depth of memory for the series A Logic Analyzer is 128K Bits in each prob.

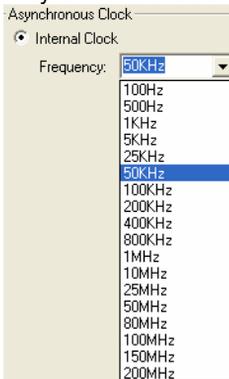
If the logic analyzer starts gathering data with a 128K memory range, it will take a long time to find the information required.

In order to avoid spending a lot of time gathering data, select a smaller RAM size. The RAM size options are 2K, 16K, 32K, 64K, 128K and 256K. So, if gathering data with 128 takes a long time why have 256K? The reason for this extra RAM size is to cope with the fact that a few of the 1~16 channels may have a large data input.

Tip:

Clock Source

Asynchronous Clock

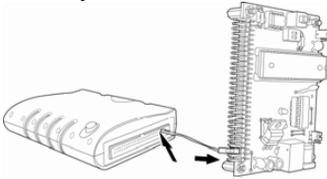


Use the drop down menu to choose the speed of the clock on the board being tested.

The sampling frequency should be more than 4 times the signal that waiting to be measured so that the waveform Duty Cycle depiction will be more accurate. Greater accuracy is acquired from the sequence of each signal between before and after occurring.

Sampling

Synchronous Clock



Choose the frequency of the clock on board the Logic Analyzer. Select “External Clock” to acquire data through External sampling. Choose either “Rising Edge” or “Falling Edge” to execute the analysis process. According to the users input the value of outdoor frequency in software; the software can count the relevant value about signal mode and frequency. For example: the value of the message, the time scale and the zoom in and out will be the value of time mode.

Connecting the Synchronous Clock

Using one of the single connecting cables put 1 end on the mother board and the other in the LA as shown in the diagram opposite.

Tip:



Compression

Check the box to compress all the data. Compression as implied by the name is used to compress acquired data through a loss less compressor. The purpose of this compression is to get more data in limited memory than in actual memory. The compressed data has a high definition without wasting any memory. The compression rate of the Logic Analyzer can be up to 255 times. This means that as the maximum acquisition can be 32M Bits (128Kx255= 32M Bits), for each channel. The chosen capacity of the memory, 1MB, means that the maximum data being sieved out arrives at 1MB*255=255M Bits (Per Channel).

Note: The rate will change depending on the data content being analyzed.

Tip:



Enable Setup

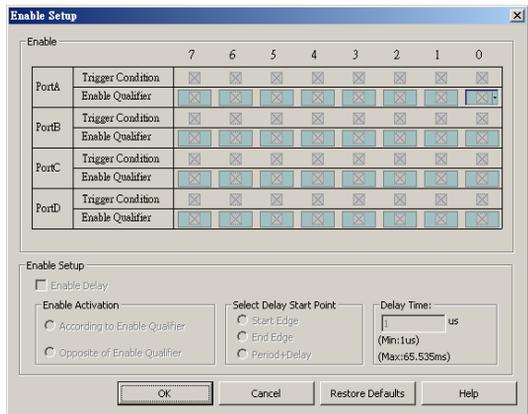


Fig 3-19: Dialogue Window: **Enable Setup**

Tip:

Click to enter the enable setup screen.

Tip:

There are 3 modes of Enable configuration for each channel.

The function of Enable is to use an alterable judgment circuit of passing signals which filter useless signals in order to capture and store valuable data in the memory. When the combination of input signals from each channel is satisfied with the condition group of "Enable Mode", the section of acquired will be gathered by the Logic analyzer and stored in the memory. After storing the data, it will return to logic analyzer's system and be displayed as a waveform. If the combination is not satisfied with the condition group, the logic analyzer won't gather and store data. So, the displayed waveform won't display this section of data.

1.  = Don't Care means capture all signals from sampling.

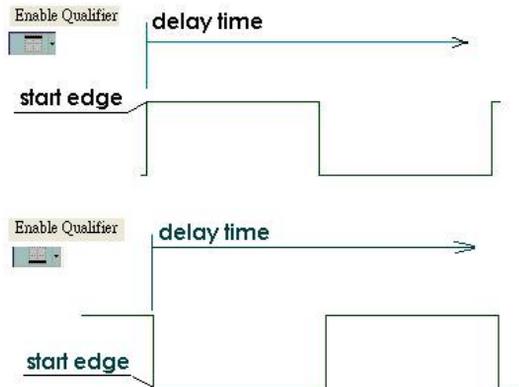


Fig 3-20 –High and Low edges

It is the system default.

2.  = High Level means that the logic analyzer captures and displays the inputting signals satisfying the high level.
3.  = Low Level, means that the logic analyzer captures and displays the inputting signals satisfying the low level.

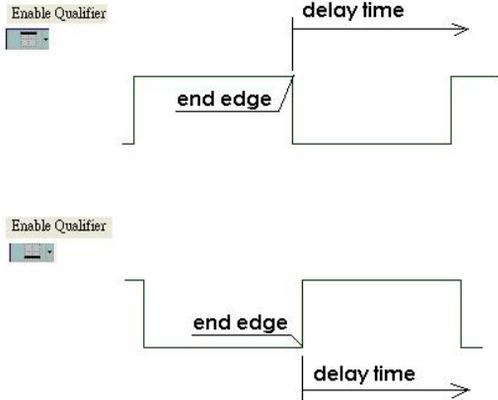


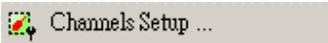
Fig 3-21 – High and Low Edge

Enable Setup

Enable Delay – according to enable qualifier.

Start Edge – Only shows the nave from start edge to delay time interval.

See details in Section 4.1.2 Tasks 1 and 2.



Tip:



Bus/Signal Setup

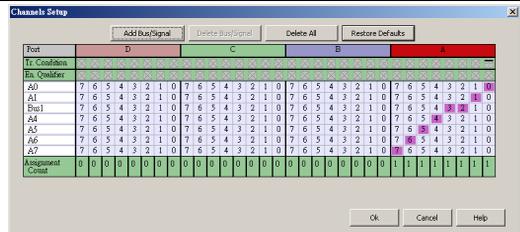


Fig 3-22: Channels Setup

See details on section 4.2

Tip:

Adding Bus/Signal

Click the **Add Bus/Signal** button to add a Port. This will appear as 'New'. Click the port(s) to be added to the new signal.

Delete Bus/Signal

Click the bus you want to delete and press the **Delete Bus/Signal** button.

Delete All

Press the **Delete All** button to delete all the buses.

Restore Defaults

Press **Restore Defaults** to return all channels and buses to the system defaults.

Group into Bus **Ctrl+G**

Signals can be **Grouped into buses** by pressing **Ctrl + G**.

Signals can be added, deleted and grouped into buses using the mouse or the keyboard or right click and select properties from the popup dialog, the functional form of sample setting. The untied Data Bus is a signal line; the signal line means Data Bus. The movement of a signal line (from over to under, hidden and display all signal line and set the character of color).

Ungroup from Bus **Ctrl+U**

Ungroup signals from buses by pressing **Ctrl + U**.

A bus contains at least 1 signal. In order to see these signals click the '+' symbol next to the name of the bus.

Expand

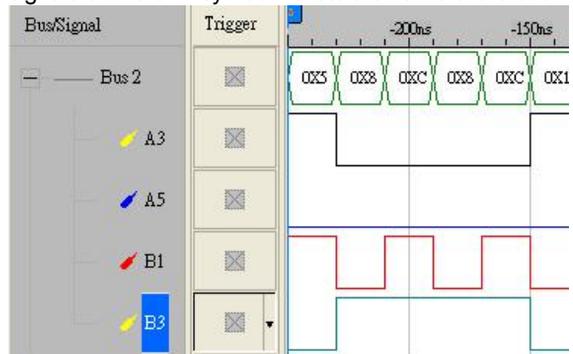


Fig 3-23 - Expand

If the bus has been expanded click the '-' symbol next to the bus name to **Collapse** the bus.

Collapse

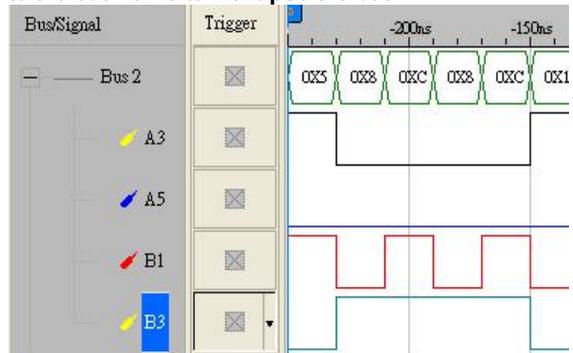


Fig 3-24 - Collapse

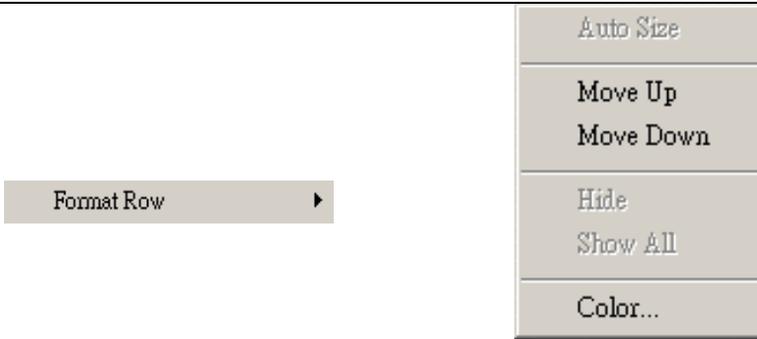


Fig 3-25 – Click to change the bus or signal display

Tip:

Format Row	Changes the display of a bus or a signal.
Autosize NOT Available in Waveform Display	Auto sizes the signal columns.
Move Up(changes to Move Left in Listing Display)	Highlight a signal or bus and click Move up (left) to move the signal or bus up (left) through the list of the bus/signal.
Move Down (changes to Move Right in Listing Display)	Highlight a signal or bus and click Move down (right) to move the signal or bus down (right) through the list of bus/signal.
Hide	Highlight a signal or bus and click hide to hide it.
Show All	Click to show all signals and busses that have been hidden.
Color	Highlight a signal or bus and click color to change the color.

Rename	Highlight a signal or bus and click Rename to rename the bus or signal.
--------	--

Trigger

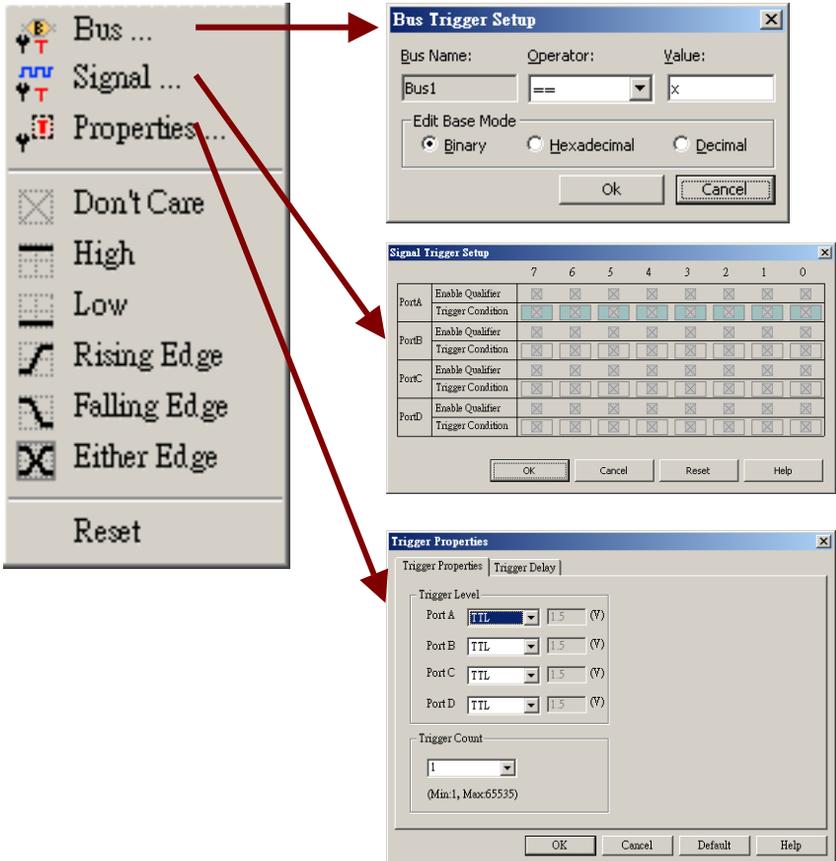


Fig 3-26: **Run/Stop** menu.



Fig 3-27: **Trigger** tool box. The 4th ~6th icons are listed in the **Trigger** menu.

Menu Bar: Trigger

Menu Item	Detail Menu or Dialogue Window
-----------	--------------------------------

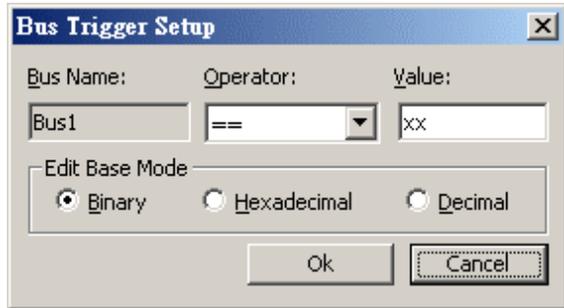


Fig 3-28: Set **Bus** triggering condition.

See section 4.2 for detailed instructions.

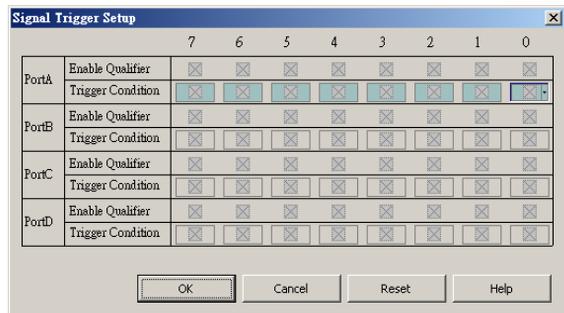
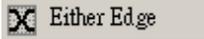


Fig 3-29: The trigger action tells the logic analyzer when to send data to the PC. The trigger conditions determine when the trigger point starts to record the information.

See sections 4.1 and 4.2 for detailed instructions.

 Don't Care	Set the trigger condition to “ Don't Care ” See section 4.1 for detailed instructions.
 High	Set the trigger condition to “ High Edge ” See section 4.1 for detailed instructions.
 Low	Set the trigger condition to “ Low Edge ” See section 4.1 for detailed instructions.
 Rising Edge	Set the trigger condition to “ Rising Edge ” See section 4.1 for detailed instructions.
 Falling Edge	Set the trigger condition to “ Falling Edge ” See section 4.1 for detailed instructions.



Set the trigger condition to **"Either Edge"**
See section 4.1 for detailed instructions.



Reset the trigger condition.

Properties ...

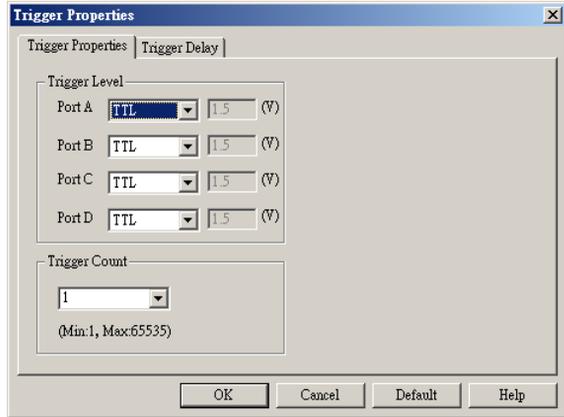


Fig 3-30: Set **Trigger Properties**.

See section 4.1 for detailed instructions.

Tips:

Trigger Content Set

Icon	Description
	Decrease trigger position
	Increase trigger position
N/A	Trigger Page
N/A	Trigger Count

Trigger Level

The voltage level that a trigger source signal must be reached before the trigger circuit initiates a sweep. There are 4 ports available, each port has the ability to assign different voltages to meet the users requirements . Use the drop down menu to choose between TTL (default TTL), (MOS L5V) – (MOS 3.3V), ECL and User Defined (Choose the value of the Trigger level – 6V to 6 V).

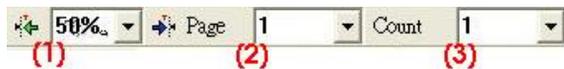


Fig 3-31: Trigger Position, Trigger page, Trigger Count

(1) Represents the Trigger Position of a memory page

(2) Represents the Trigger Page.

(3) Represents the Trigger Count.

Tip:

Trigger Delay

Icon	Description
N/A	Trigger Delay Clock

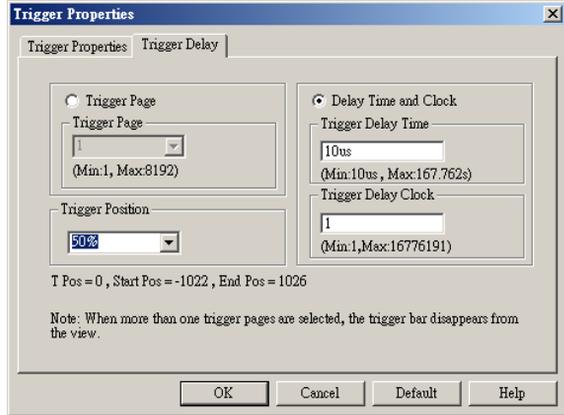


Fig 3-32: Set **Trigger Delay**.

See section 4.1 for detailed instructions.

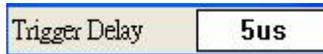


Fig 3-33: Setup **Trigger Delay** clock under time mode.

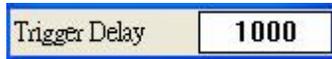


Fig 3-34: Setup **Trigger Delay** clock under address mode.

The **Trigger Delay** in **Trigger Delay Tool Box** equals to the **Trigger Delay Clock** in the above dialogue window.

Run/Stop



Fig 3-35: **Run/Stop** menu.

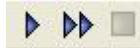


Fig 3-36: **Run/Stop** tool box.

Menu Bar: **Run/Stop**

Menu Item	Detail Menu or Dialogue Window
▶ Single Run F5	Click to run once. See section 4.1.1 for detailed instructions.
▶▶ Repetitive Run F6	Click to run continuously until the stop button is pressed. See section 4.1.1 for detailed instructions.
■ Stop F7	Click to Stop the retentive run. See section 4.1.1 for detailed instructions.

Menu Bar: Data

Menu Item

Detail Menu or Dialog Window

Select Analysis Range

Check the box to enable the Analytical range to be changed by dragging the Ds and Dp holders with the left mouse button.

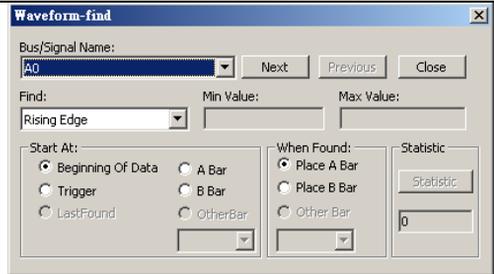


Fig 3-39: Find Data Value
from a signal or bus.

See Chapter 4 for detailed instructions.

Using the drop down menu select the Bus / Signal Name:

 Find Data Value ... **Ctrl+F**

Choose which attribute to find. The list of attributes depends on whether it is a Bus or Signal that is being searched in: Bus – Choose between ==, Not=, In Range, Not in Range (enter the value for Min Position and max Position). Signal – Choose between Rising Edge, Falling Edge, Either Edge, High, Low. Choose where to **Start** our search by selecting one of the following:

Beginning of Data, Trigger, Last Found (based on the previous search), A Bar, B Bar, and Other Bar (select from the drop down menu).

When Found choose whether to place the following: A Bar, B Bar, Other Bar (if available from the drop down list) Statistic – Shows the number of instances of the search results.

Note: Only applicable when search through a bus.

 Before **F11**

Go to previous edge sweep of the signal indicated.

 After **F12**

Go to next edge sweep of the signal indicated.

GoTo

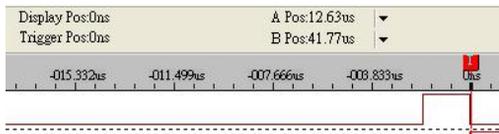
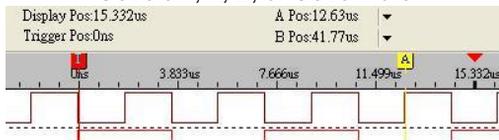
GoTo a T, A, B, or GoTo More


Fig 3-40: T Bar will be displayed in the center of the wave area.

Tip:


- ① Press T, go to Trigger bar.
- ② Press A, go to A bar.
- ③ Press B, go to B bar.

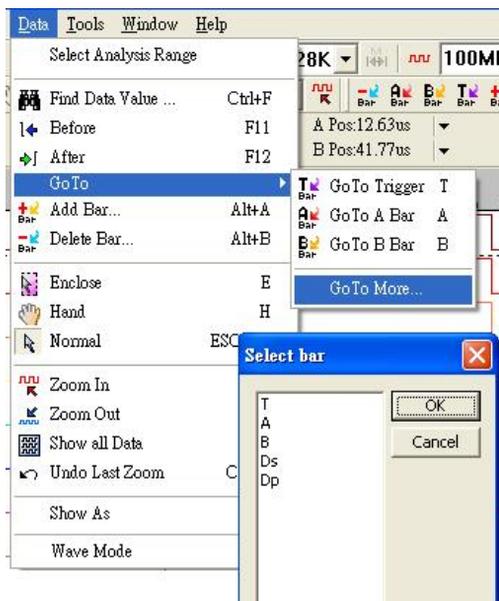


Fig 3-41: The selected bar will be shifted to center of wave area.



Add an user defined bars.

1. Click the above menu item from **Data** menu, or click **Add Bar** icon from **Tool Bar**.
2. Give a **Bar Name**, define a **Bar Color**, and, perhaps, a **Bar Position**.

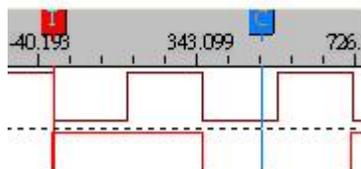
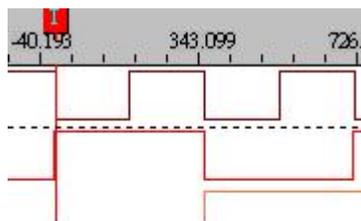
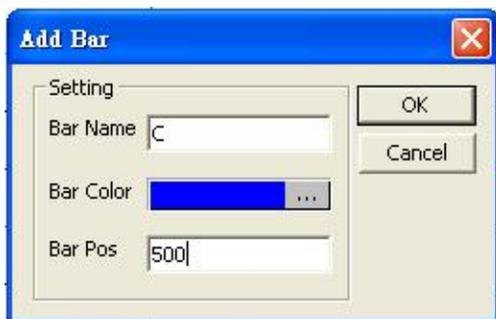


Fig 3-42: Equivalent feature listed on Tool Bar/Box.



Delete a user defined bars.

1. Click the above menu item from **Data** menu, or click **Delete Bar** icon from **Tool Bar**.
2. Select a user defined bar, and click on **Delete**.

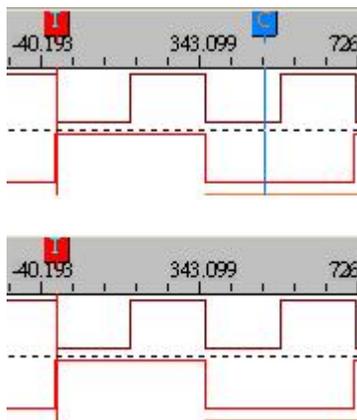
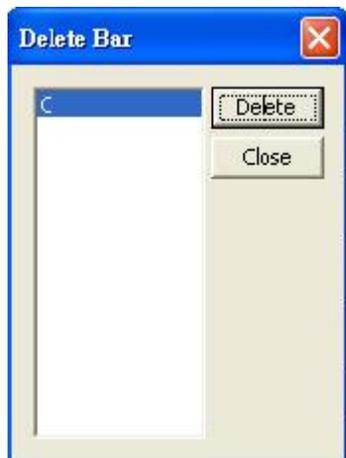


Fig 3-43: Delete a selected **Bar**.

 Enclose E

A Zoom-In or a Zoom-Out view will be centered in the Position Display Area, and the new zoomed view will be either extended to the dimension of the Position Display Area or shrink according to the relative ratio to the Position Display Area.

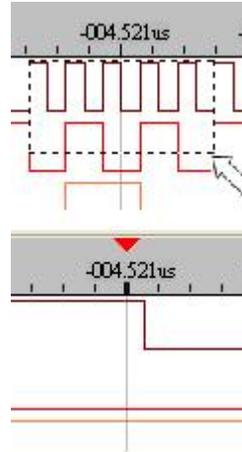


Fig 3-44: To **Zoom Out**, left click and drag the mouse/point from left to right direction.

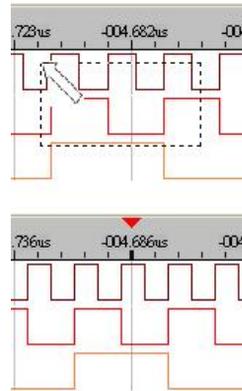


Fig 3-45: To **Zoom In**, left click and drag the mouse/point from right to left direction.

 Hand H

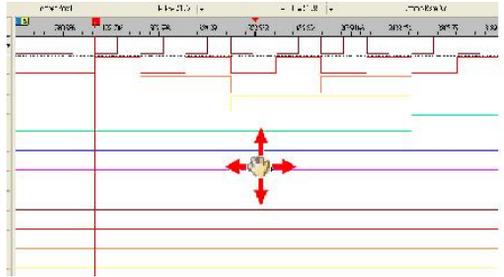


Fig 3-46: Click Hand, and then press the left mouse button to drag around the page.

 Normal ESCAPE

Reset the mouse / pointer function to system default.

To have a closer view (**Zoom In**) or broader view (**Zoom Out**)

	Zoom In	F9
	Zoom Out	F8

Notes on zooming:

Zooming in and out can be switched by the proportion and time mode that embodies the pull-down function.

1. The switch of zooming in and out means exchanging the display of message mode.

Address: The proportion module

Time and Frequency: Time module.

2. The system can set the value of zooming in and out:

The default unit is us when zooming out it will automatically reduce to ns. When zooming in it will increase in increments to ms, s and ks.

3. Pull-down menu:

There are thirty scales. At first, define each grid as the quantity of the cycle and exchange it to become the proportion and the time.

The maximum zoom in and out is the cycle of each grid, 0.0001piece.

The minimum zoom in and out is the cycle of each grid, 1,000,000,000.

Zoom in and out (the proportion): with each grid being the cycle, the zoom in and out (%) is 100%. The time of zoom in and out counts by the clock of each grid (sample frequency). For example:

(1) Each grid is being a cycle; the zoom in and out is 100%. The time of zoom in and out will be presented by the clock of each grid X (1/sample frequency)

(2) Each grid stands for the clock of 100 pieces, the zoom in and out is 1% and the time of zoom in and out will be displayed by the cycle of each grid, X (1/sample frequency)

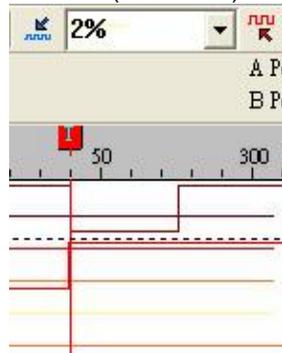


Fig 3-47: Normal status

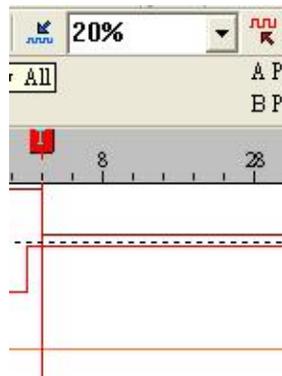


Fig 3-48: Result from normal to **Zoom In**

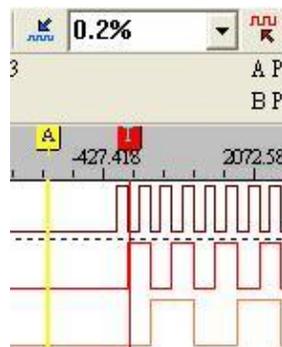


Fig 3-49: Result from normal to **Zoom Out**

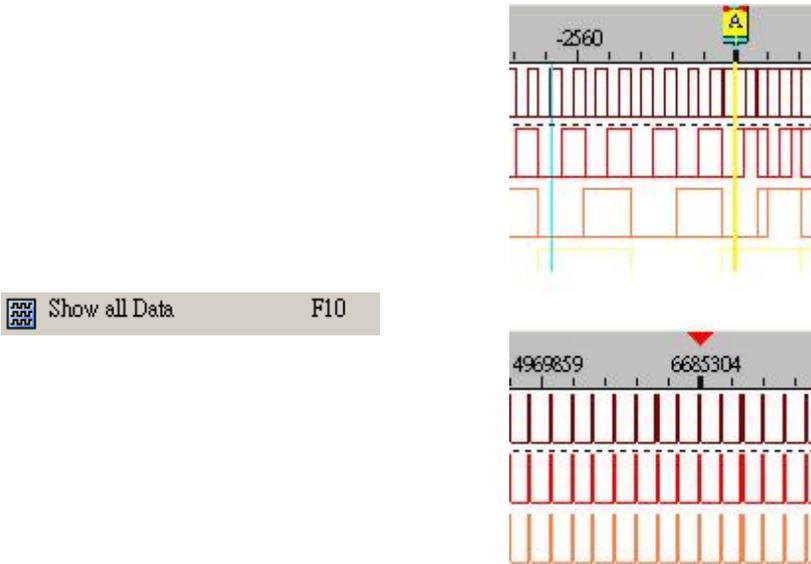
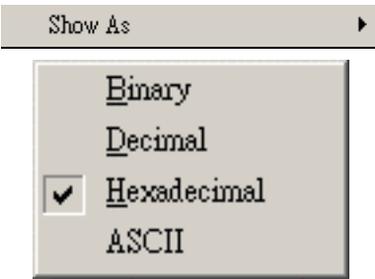


Fig 3-50: **Show all Data** of a memory page



Undo the last Zoom.



Show numerical information in binary, decimal, hexadecimal, or ASCII

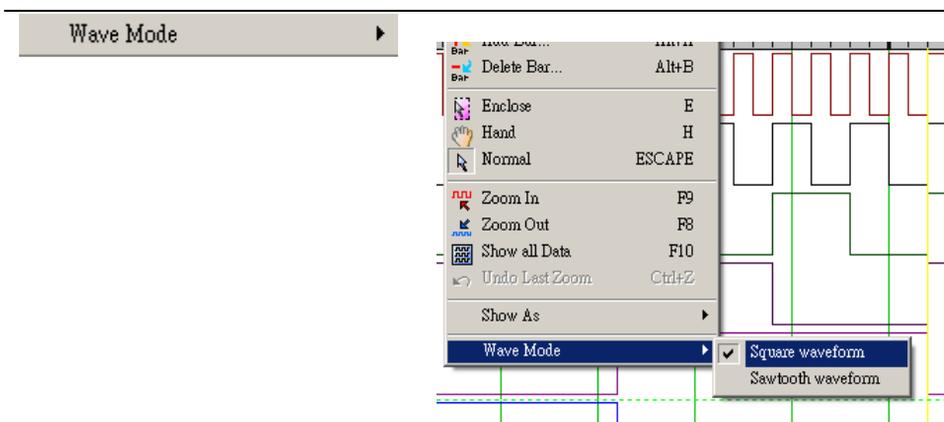


Fig 3-51: **Wave Mode** in the Square waveform.

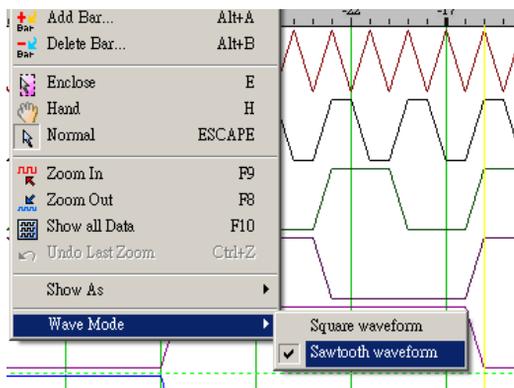
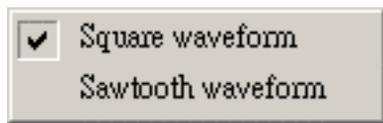


Fig 3-52: **Wave Mode** in the Saw tooth waveform.

Tools

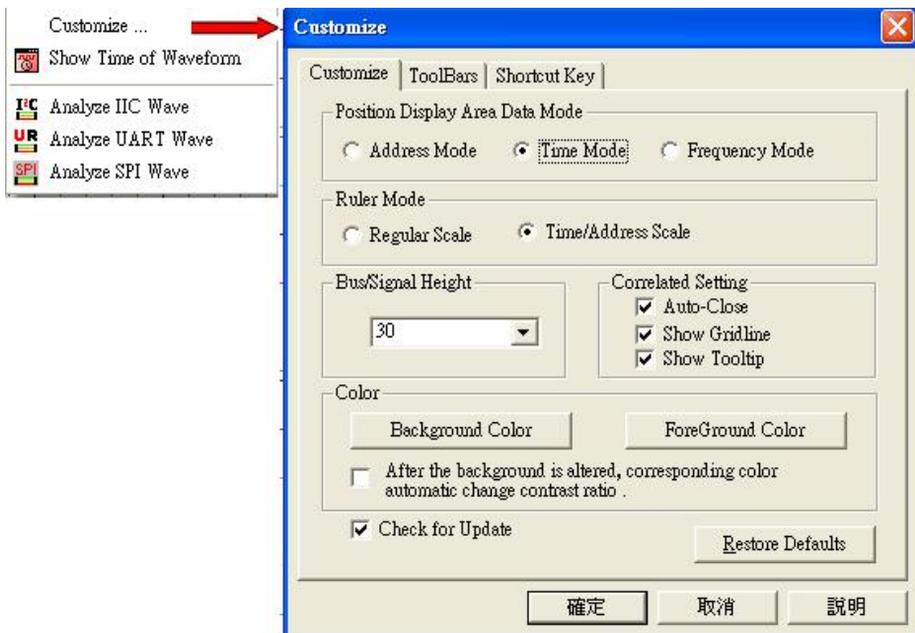


Fig 3-53: **Tools** menu.

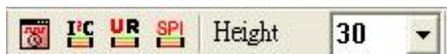


Fig 3-54: **Mouse Pattern** tool box.

Menu Bar: Tools

Menu Item

Detail Menu or Dialogue Window

Customize ...

See Section 3.4 for detailed instructions.



Fig 3-55: Customize the workspace.



Fig 3-56: Customize tool bars

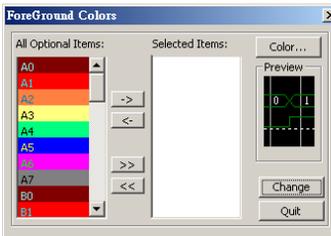


Fig 3-57: Customize shortcut key

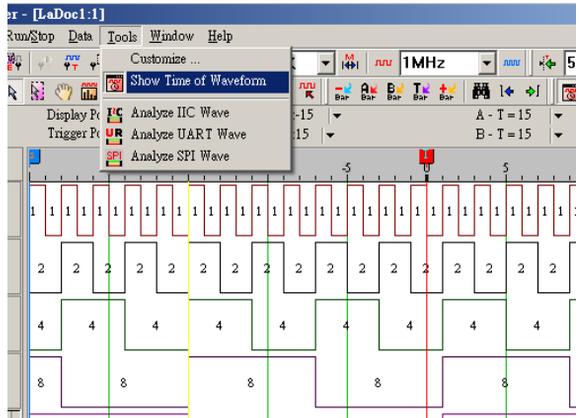
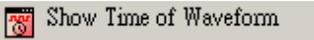


Fig 3-58: Show Time of Waveform
under address mode.



Show Time of Waveform

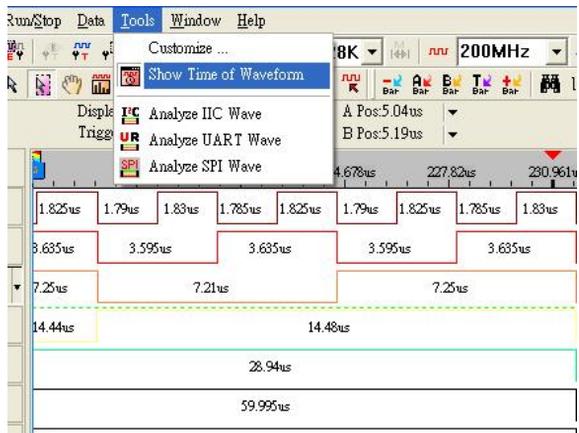
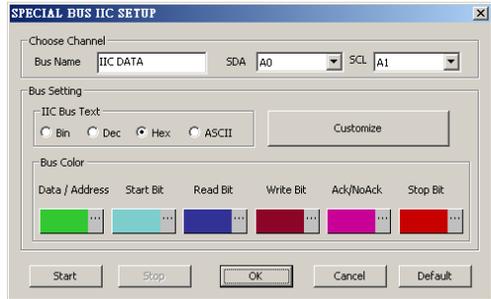
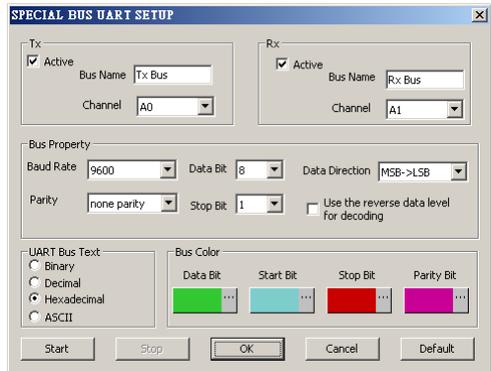


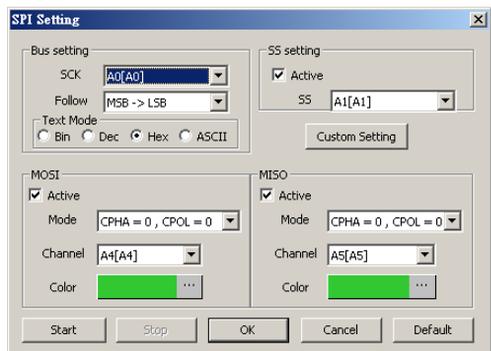
Fig 3-59: Show Time of Waveform
under time mode.


Analyze IIC Wave

Fig 3-60: Analyze IIC Wave.

See section 4.3 for detailed instructions.


Analyze UART Wave

Fig 3-61: Analyze UART Wave

See section 4.45 for detailed instructions.


Analyze SPI Wave

Fig 3-62: Analyze SPI Wave.

See section 4.5 for detailed instructions.

Window

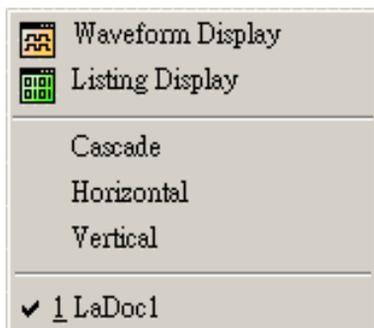


Fig 3-63: **Window** menu.



Fig 3-64: **Window** tool box.

Menu Bar: Windows

Menu Item

Detail Menu or Dialogue Window

 Waveform Display

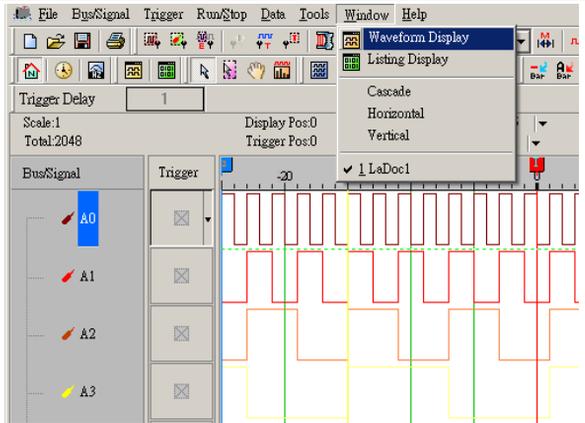


Fig 3-65: Display signals in Waveform.

 Listing Display

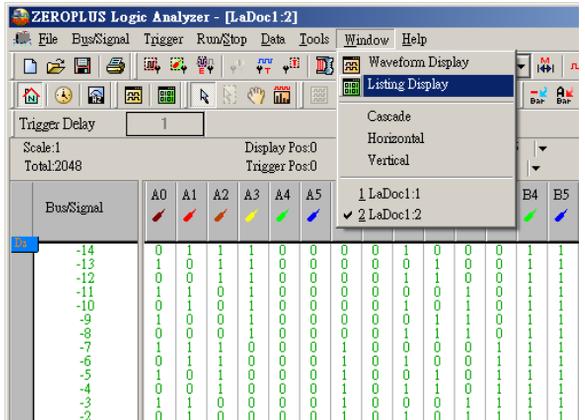


Fig 3-66: Display signals in Listing.

Cascade

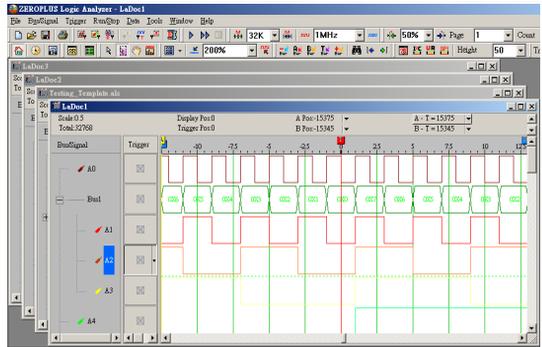


Fig 3-67: Cascade workspace(s)

Horizontal

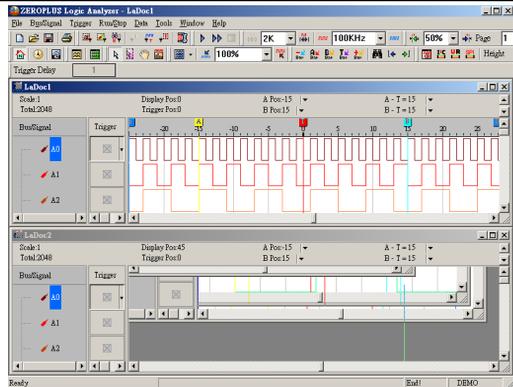


Fig 3-68: Align workspace(s) Horizontally.

Vertical

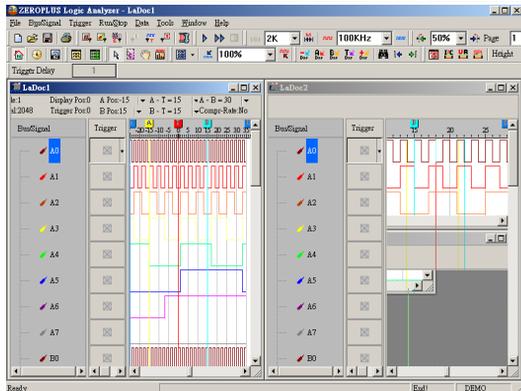


Fig 3-69: Align workspace(s) Vertically.

Help

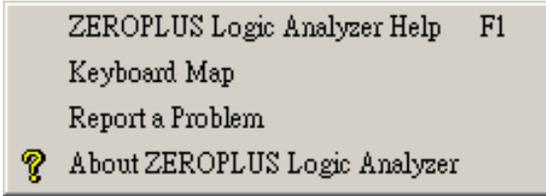


Fig 3-70: **Help** menu.

Menu Bar: Help

Menu Item

Detail Menu or Dialogue Window

Logic Analyzer Help F1



Fig 3-71: Open **Logic Analyzer Help** file.

Keyboard Map

Orders	Hot key	
Place the A Bar position	A	Move waveform to where takes A-t
Place the B Bar position	B	Move waveform to where takes B-t
Place the T Bar position	T	Position T-Bar to the center of disp
Change to Enclose mode	E	Change the mouse mode to Encl
Change to Hand mode	H	Change the mouse mode to Hand.
Put A Bar	Ctrl + A	Put A-Bar on the center of display
Put B Bar	Ctrl + B	Put B-Bar on the center of display
File -> Graph	Ctrl + C	Open the dialogue of Capture Grap
Data -> Enclose	Ctrl + E	To transfer the mode of mouse is t
Data -> Find Data Value	Ctrl + F	Search specific data with predeter
Bus/Signal -> Group into Bus	Ctrl + G	Group selected signals into Bus
File -> New	Ctrl + N	Create a new file
File -> Open	Ctrl + O	Open saved file

 Fig 3-72: The table of **Keyboard Map**.

Report a Problem

Report a Problem to the service e-mail at
service_2@zeroplus.com.tw

 **About Logic Analyzer**

 Fig 3-73: Copyright **About Logic Analyzer**.

3.2 Find Data Value

Find Data Value is a very useful tool to help the user to find data on the signals received.

- Step 1.** Click the find data value  icon, the dialogue of Waveform find will appear.
- Step 2.** Using the drop down menu select the Bus/Signal Name.
 The Bus/Signals listed on the drop down menu represent the status of the Bus/Signal column as shown in Fig 3-74.

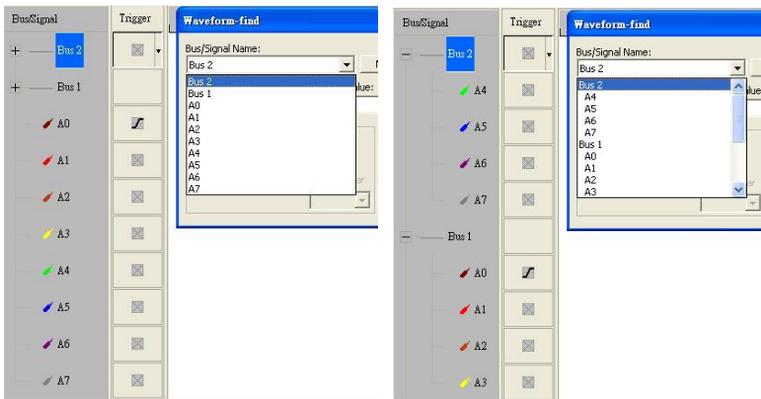


Fig 3-74

- Step 3.** Choose which attribute to find. The list of attributes depend on whether it is a Bus or Signal or the special protocol bus such as IIC/ UART/ SPI...etc that is being searched in, see Figs 3-75, 3-76, 3-77, 3-78, 3-79, 3-80, 3-81 and 3-82.

Bus: Choose between =, Not, In Range, Not in Range (enter the Min Position or Max Position values).

Special protocol Bus: Choose the segments bits of the bus (enter the value for Min Position or Max Position).

Signal: Choose between Rising Edge, Falling Edge, Either Edge, High or Low.

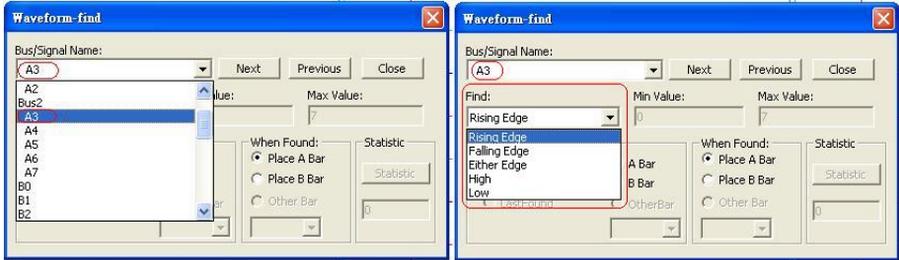


Fig 3-75: Waveform-find Dialogue of the Logic Signal

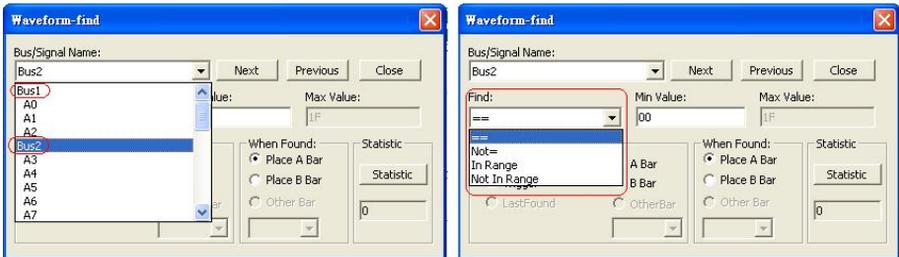


Fig 3-76: Waveform-find Dialogue of the Logic bus

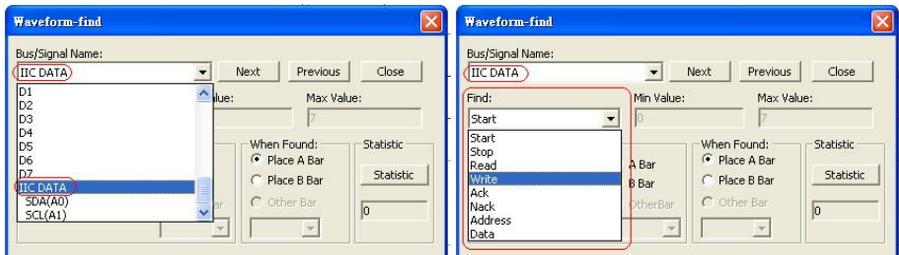


Fig 3-77: Waveform-find Dialogue of the IIC bus

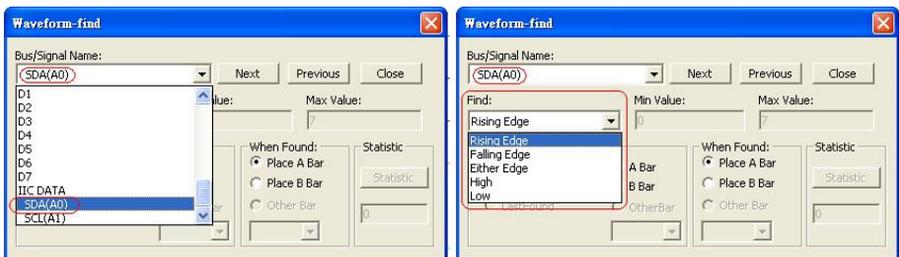


Fig 3-78: Waveform-find Dialogue of the IIC signal

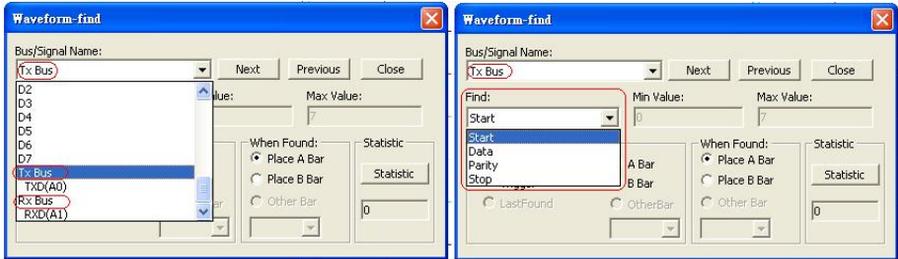


Fig 3-79: Waveform-find Dialogue of the UART bus

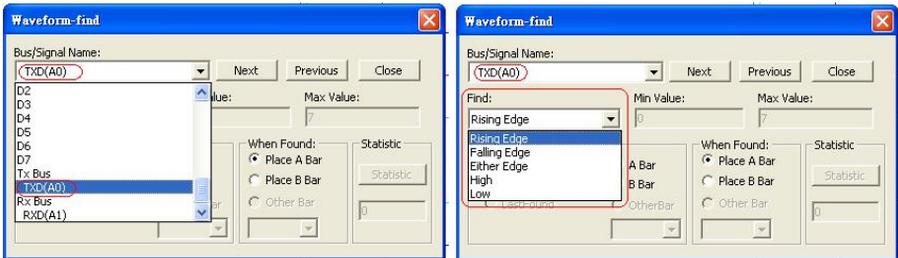


Fig 3-80: Waveform-find Dialogue of the WART signal

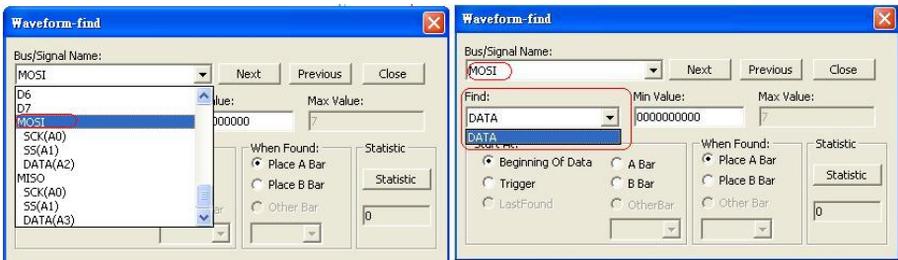


Fig 3-81: Waveform-find Dialogue of the SPI bus

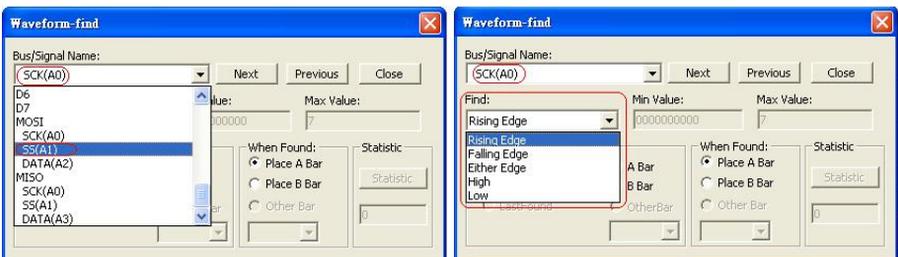


Fig 3-82: Waveform-find Dialogue of the SPI signal

Step 4. Choose where to Start the search by selecting one of the following: Beginning of Data, Trigger, Last Found (based on the previous search), A Bar, and Other Bar (select from the drop down menu), then click Next or Previous to search it.

When Found choose whether to place the following: A Bar, B Bar, Other Bar (if available from the drop down list)

Step 5. Click Statistic to show the number of instances of the search results.

Note: This is only applicable when searching through a bus.

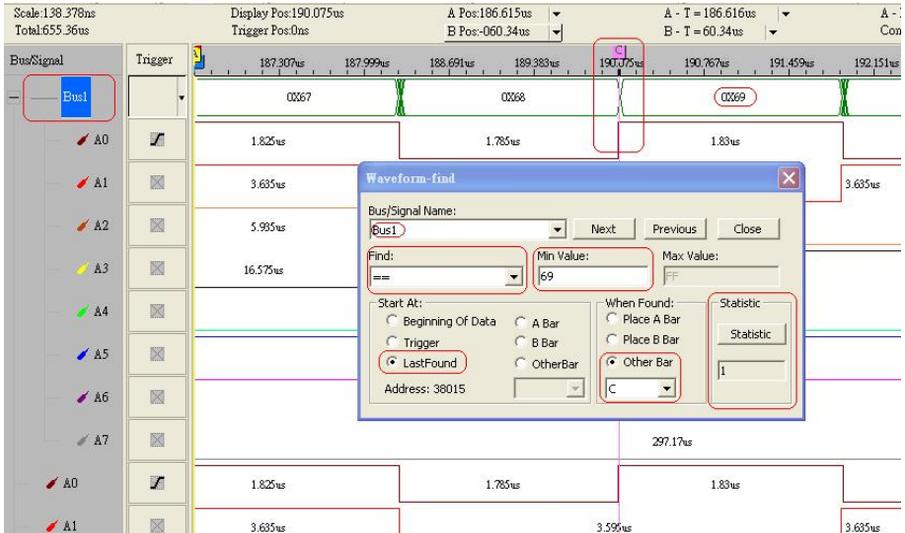


Fig 3-83: The C bar is placed at the 0X69 of Bus1 where the condition of the Waveform-find is set. The Statistic of Waveform-find shows a “69” on Bus1.

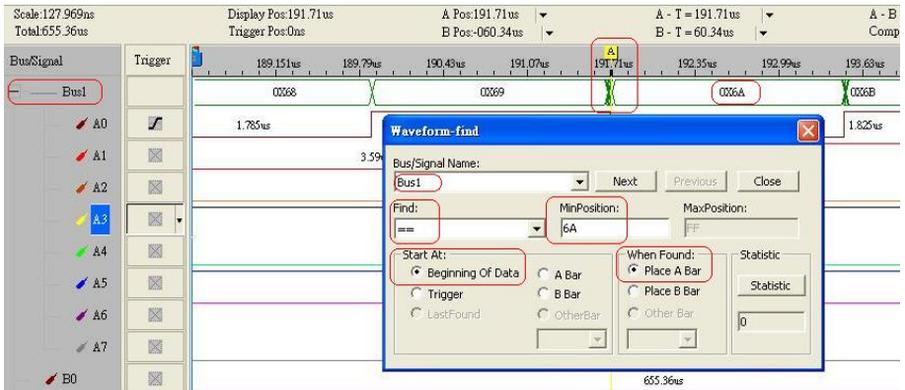
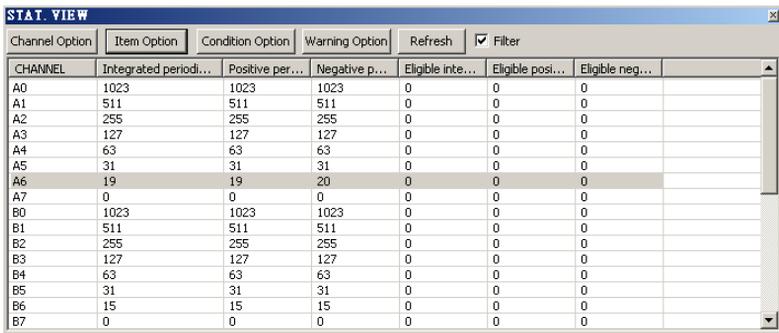


Fig 3-84: The A bar is placed at the 0X6A of Bus1 where the condition of the Waveform-find is set.

3.3 Statistics Feature

Section 3.3 presents detailed information on the **Statistics** feature in the software interface. The **Statistics** feature presents user information pertaining to six periodicities: **Integrated Periodicities**, **Positive Periodicities**, **Negative Periodicities**, **Eligible Integrated Periodicities**, **Eligible Positive Periodicities**, and **Eligible Negative Periodicities**.

Click on the **Statistics** icon  and an interface like Fig 3-85 or Fig 3-86 will prompt.



Channel Option	Item Option	Condition Option	Warning Option	Refresh	<input checked="" type="checkbox"/> Filter	
CHANNEL	Integrated periodi...	Positive per...	Negative p...	Eligible inte...	Eligible posi...	Eligible neg...
A0	1023	1023	1023	0	0	0
A1	511	511	511	0	0	0
A2	255	255	255	0	0	0
A3	127	127	127	0	0	0
A4	63	63	63	0	0	0
A5	31	31	31	0	0	0
A6	19	19	20	0	0	0
A7	0	0	0	0	0	0
B0	1023	1023	1023	0	0	0
B1	511	511	511	0	0	0
B2	255	255	255	0	0	0
B3	127	127	127	0	0	0
B4	63	63	63	0	0	0
B5	31	31	31	0	0	0
B6	15	15	15	0	0	0
B7	0	0	0	0	0	0

Fig 3-85: STAT. VIEW.

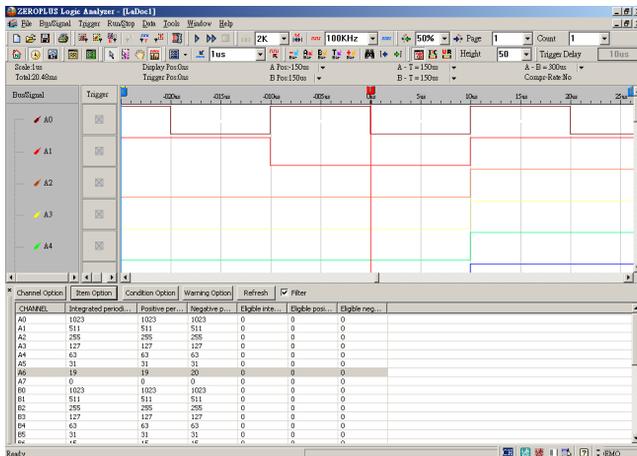


Fig 3-86: Logic Analyzer with statistics enabled.

There are four options for adjusting how statistical information may be presented. These four options are **Channel Option**, **Item Option**, **Condition Option**, and **Warning Option**.

Channel Option

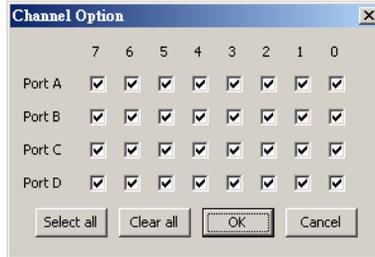


Fig 3-87: **Channel Option**. Allows the choice of which pin in which port will be included in the statistical analysis of a test run.

Item Option

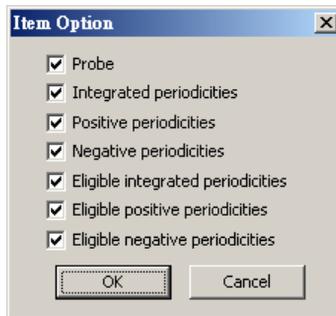


Fig 3-88: **Channel Option**. Allows choice of what periodicities will be considered in statistical results

Conditions Option

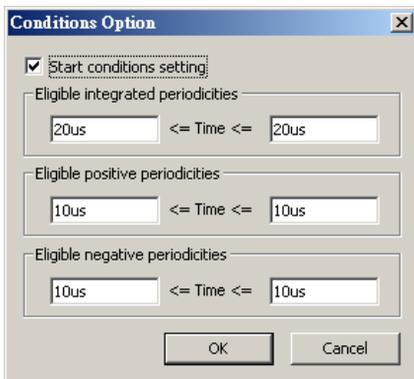


Fig 3-89: **Conditions Option** allows configuring of time intervals for Eligible Integrated, Eligible Positive and Eligible Negative Periodicities.

CHAN...	Integrate...	Positive pe...	Negative pe...	Eligible integ...	Eligible posit...	Eligible...
A0	127	127	127	126	127	126
A1	65	65	66	65	65	65
A2	33	33	34	33	33	33
A3	16	16	17	16	16	16
A4	8	8	9	0	0	1
A5	4	4	5	0	0	0
A6	2	2	3	2	0	0
A7	1	1	2	1	1	1
B0	0	0	1	0	0	1
B1	0	0	1	0	0	1

Fig 3-90: The numbers of waves qualified by conditions set.

Warning Option

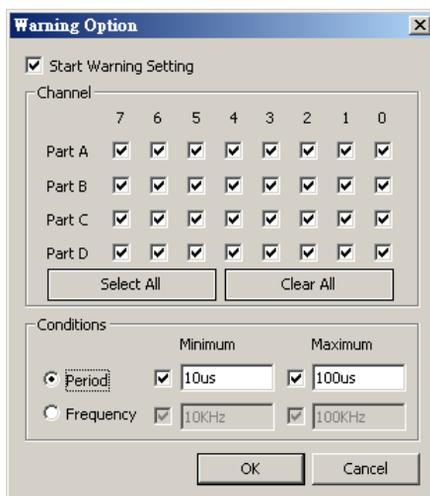


Fig 3-91: **Warning Option** allows choice of pin and port.

CHAN...	Integrate...	Positive pe...	Negative pe...	Eligible integ...	Eligible posit...	Eligible...
A0	127	127	127	126	127	126
A1	65	65	66	65	65	65
A2	33	33	34	33	33	33
A3	16	16	17	16	16	16
A4	8	8	9	0	0	1
A5	4	4	5	0	0	0
A6	2	2	3	2	0	0
A7	1	1	2	1	1	1
B0	0	0	1	0	0	1
B1	0	0	1	0	0	1

Fig 3-92: The numbers of waves qualified by conditions settled are printed in black, otherwise in red.

3.4.1 Modify Display Mode

To modify the display mode, users may use icons on the tool bar/box, or menu. For the menu, go to **Tools** and click **Customize**. See Fig.3-94.

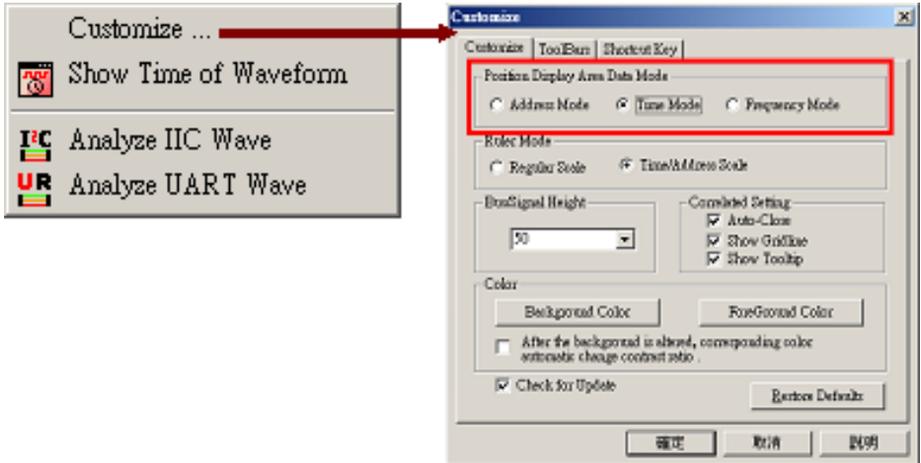


Fig 3-94: Customizing the display by using the tool bar (see Figs 3-95 and 3-96)

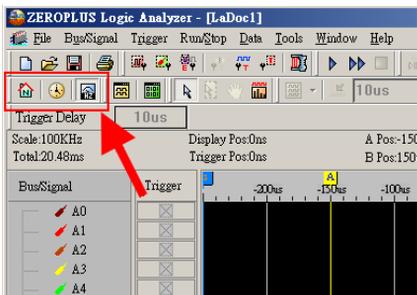


Fig 3-95 – Tool bar

-  Address Mode
-  Time Mode
-  Frequency Mode



Fig 3-96 – Toolbar detail

Position Display Area Data Mode – There are 3 modes to determine the method of capturing data from sampling: Address Mode, Time Mode, Frequency Mode

3.4.2 Modify Ruler Mode

To modify the Ruler mode, use the menu.

Go to **Tools** and click **Customize**. See Fig. 3-97

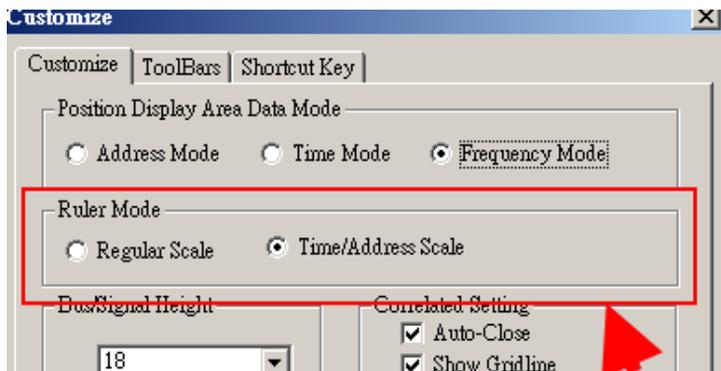


Fig 3-97 – Ruler Mode

Regular Scale



Fig 3-98: Ruler in Regular Scale

Time/Address Scale



Fig 3-99: Ruler in Time/Address Scale

Ruler Mode – Divided into two styles of scale: (Regular scale, Time and address)

Regular Scale:

Presented on increments of 5.

Time/Address scale (default):

Presented in increments of 100us.

3.4.3 Modify Bus/Signal Height & Correlated Setting

To modify Bus/Signal Height, click **Tools** → **Customize**.

Bus/Signal Height Set the height of waveform (18-100) in chosen items at toolbar that will show the amplitude of the waveform.

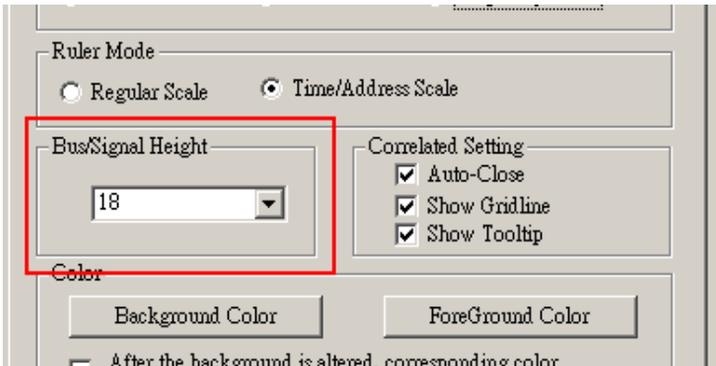


Fig 3-100 – Bus/Signal Height

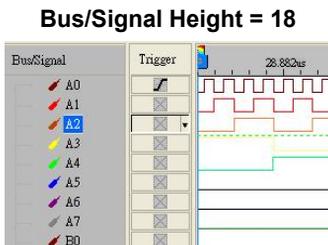


Fig 3-101-1

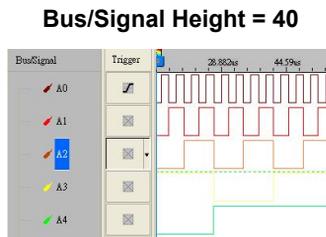


Fig 3-101-2

Fig 3-101 – Examples of Bus/Signal Height

Correlated Setting

Check the boxes to activate the following settings.

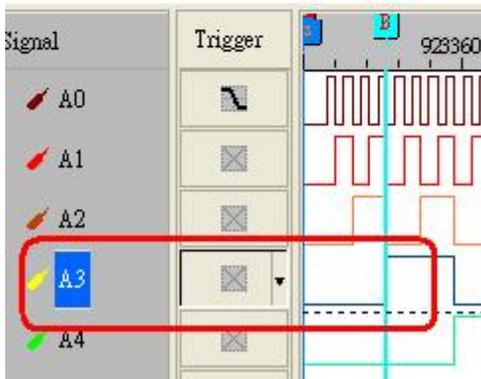
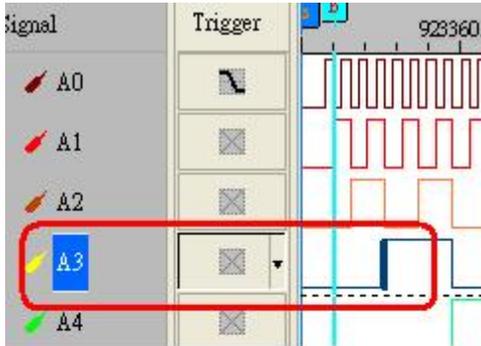


Fig 3-102 – Auto Close

Auto Close - With the cursor in the channel, the Bar will close it by the edge of the approaching channel (High edge or Low edge).

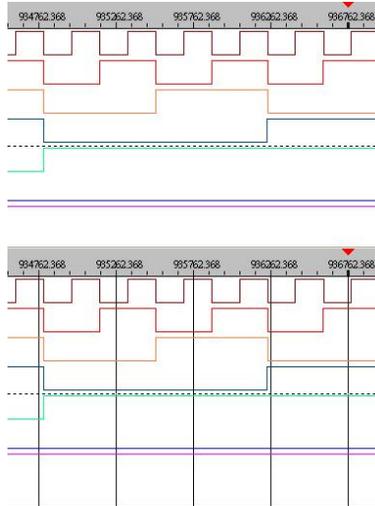


Fig 3-103 - Gridlines

Show Gridline - The gridlines will be displayed in the waveform display

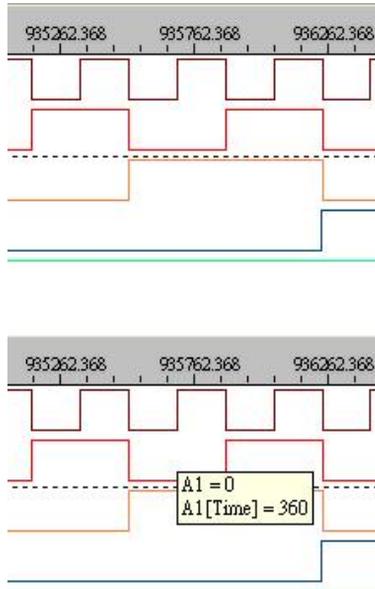


Fig 3-104 - Tooltips

Show Tooltip – Leave the mouse over an icon or a wave and the description will be shown.

3.4.4 Modify Color

To modify Bus/Signal Height, click **Tools → Customize**.

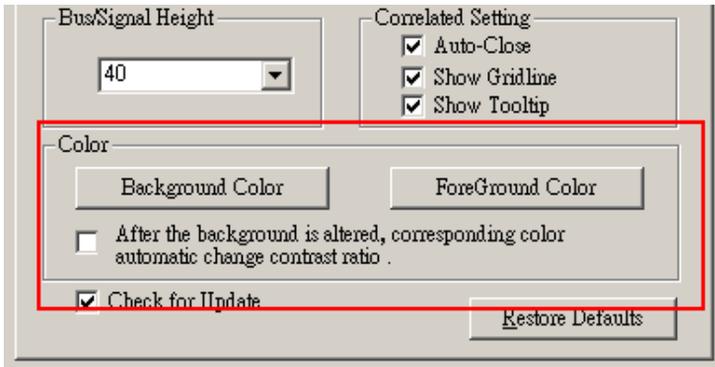


Fig 3-105– Background and Foreground color buttons

Background Color – The background color of the Logic analyzer.



Fig 3-106 – Background Color Menu

Wave BackGround: The logic Analyzers Waveform Viewer BackGround Color.

List BackGround Color1: The logic Analyzers Listing Viewer First BackGround Color.

List BackGround Color 2: The logic Analyzers Listing Viewer Second BackGround Color.

Note: Two colors are displayed in the Listing display

Foreground Color – Changes the color of the text and waves.

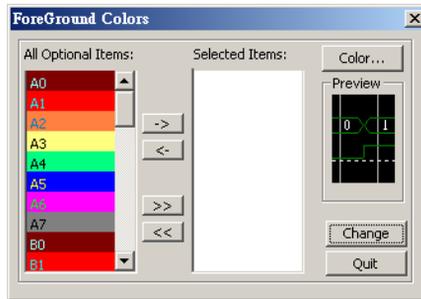


Fig 3-107 – Foreground Color Menu

All Optional Items: All Optional Items includes the current color of all Bus, signals, Cursors , grids, unknown lines, default bus, Bus text and List text (You can roll the vertical reel to view the selecting items).

Selected items: You can configure the color of Bus, Signals, Cursors, grids, unknown lines, default bus, Bus text and List text.

Color: There are 48 basic colors available for Selected Items.

Change: Click “Change” to alter the selected Items’ color.

Quit: Quit the dialogue of Foreground Colors and return to customize dialogue.

After the background is altered, corresponding color automatic change contrast ratio – When the users set the color of background that chooses the corresponding color or the system will switch automatically to become the contrast color.

Check for up Update: The Logic analyzer software will automatically check for updates when being started.

Restore Defaults: Background color, waveform color, cursor color, script color, grid type and bus color return to the initial setting.

3.4.4.1 Modify Background Color

To modify Background Color, click the color block shown in Fig 3-108. A **Color** panel, shown in Fig 3-109, will prompt users. Select a color shown on the panel or click on **Define Customized Color** to create your own.

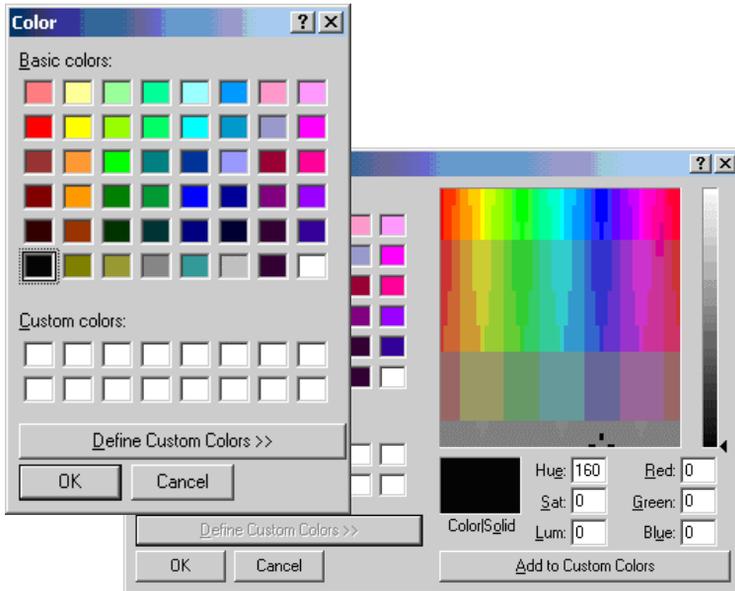


Fig 3-108: **Color** panel with its advance view.

3.4.4.2 Modify Foreground Color

Foreground color refers to the color of the output signal lines in the Position Display Area. Fig. 3-109 presents how to change color of a signal. Repeat the following procedures if requiring to change colors of multiple items.

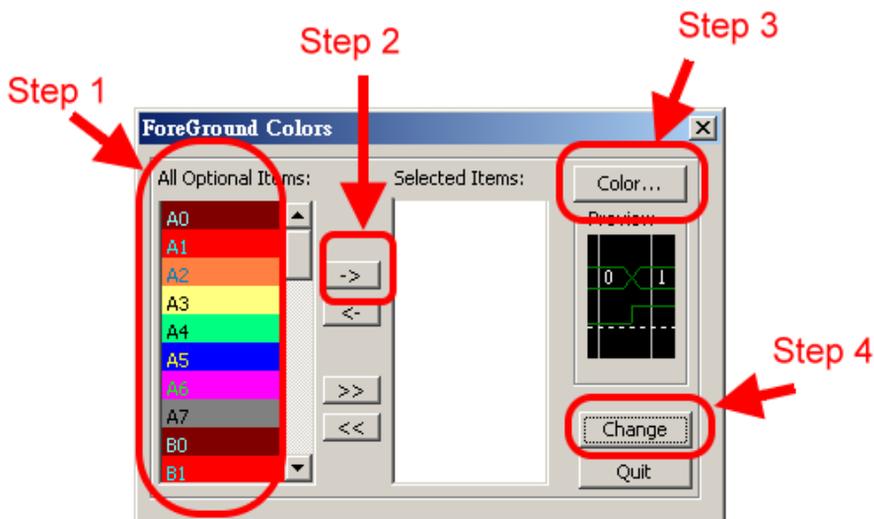


Fig 3-109: Stepwise illustration of changing **Foreground Colors**

Step 1: Select an **Optional Item**.

Step 2: Click the -> and the item will appear in **Selected Items**.

Step 3: Choose a color by following the method shown in Fig 3-88.

Step 4: Click **Change** to apply the color change.

Here is a sample of an altered Logic Analyzer software interface which will be used for further demonstrations in subsequent chapters. See *Fig 3-110*

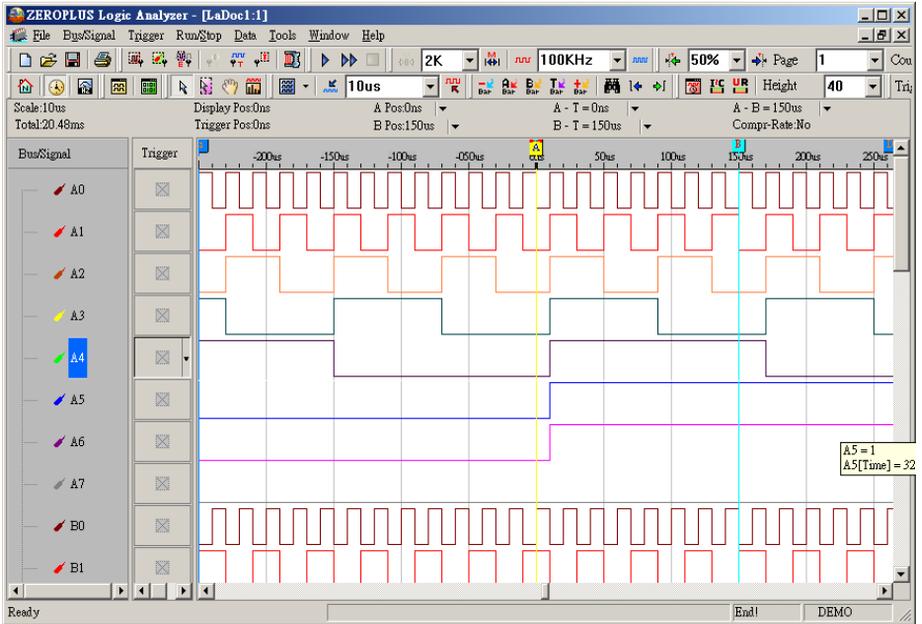


Fig 3-110: Sample altered interface to be used in subsequent chapters.

3.5 The flow of software operation

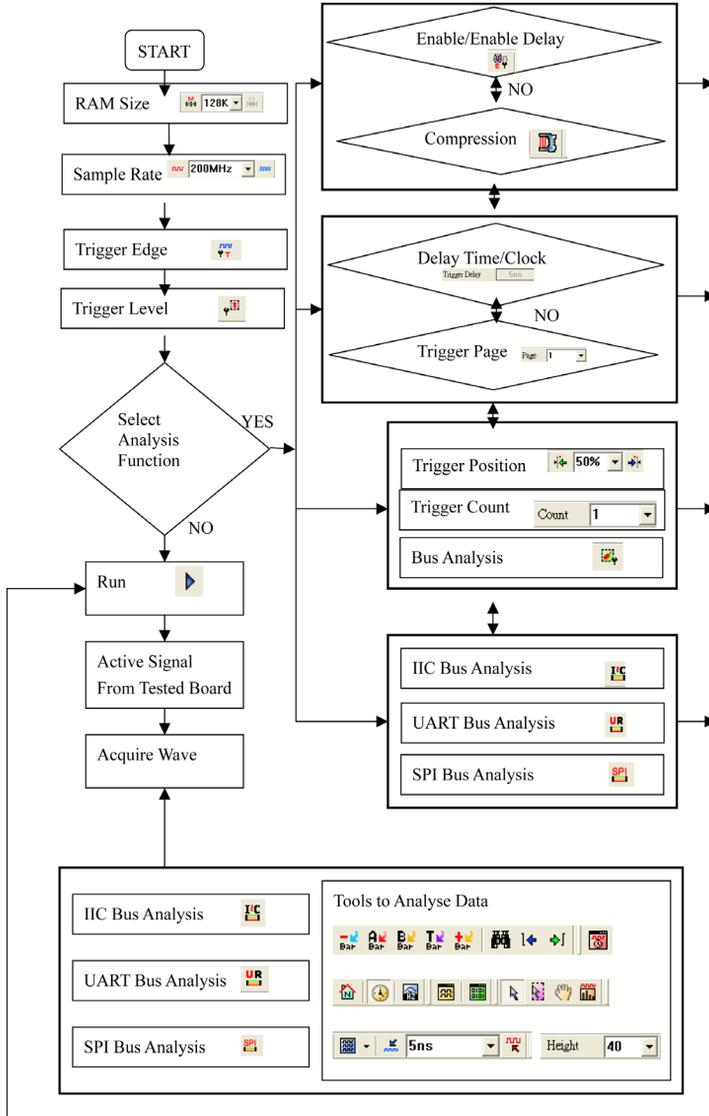


Fig 3-111 – Software Flow Diagram

Conclusion

Information demonstrated in this chapter is only for entrance level. There are more advanced approaches which may require fewer steps than those shown in this chapter. This chapter is meant to equip users with sufficient grounding of the Logic Analyzers software interface. The same contents will now be repeated, if they are not crucial. We advise repeat readings of this chapter.

4 Introduction to Logic Analysis

- 4.1 The Logic Analysis
- 4.2 The Bus Logic Analysis
- 4.3 The IIC Analysis
- 4.4 UART Analysis
- 4.5 The SPI Analysis
- 4.6 Compression
- 4.7 Enable and Enable Delay

Objective

Chapter 4 gives detailed instructions in performing two basic analysis operations and five advance analysis applications with the Logic Analyzer. These two basic analytical operations are the Logic Analysis and the Bus Analysis, which are fundamental to all further applications. The other five advance analytical applications are the IIC (Inter Integrated Circuit) Analysis and the UART (Universal Asynchronous Receiver Transmitter) Analysis, the SPI (Synchronous Peripheral Interface) Analysis, the Compression, and the Enable and Enable Delay.

4.1 The Logic Analysis

Logic Analysis is meant for a single signal analysis. Section 4.1 gives detailed instructions on the software's basic setup.

Basic Software setup of the Logic Analysis

Task 1. Clock Source (Frequency) and RAM Size set up

Step 1. Click  icon or Click Sampling Setup from Bus/Signal on the menu bar, the dialogue as shown in Fig 4-1 will appear.

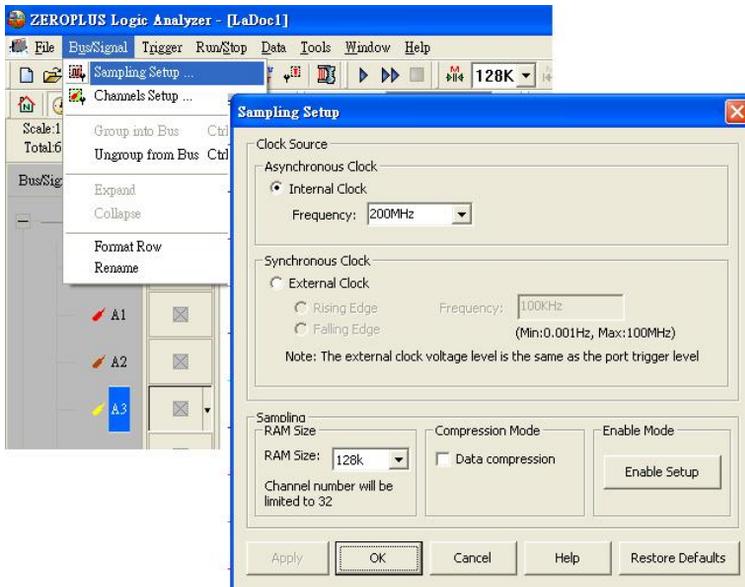


Fig 4-1 – Clock Source

Step 2. Internal Clock (Asynchronous Clock)

Click on Internal Clock, and then select the Frequency from the pull down menu to set up the Frequency of tested circuit board. The frequency of the Internal Clock must be At Least Four Times Higher then the frequency of the Oscillator on the tested board. Or Select the Frequency  from the pull down menu on Tool Bar as Fig 4-2 shows.

Tip: Connect the output pin of the oscillator from the tested board to the Signal connector of Logic Analyzer to measure it using the internal clock of Logic Analyzer.

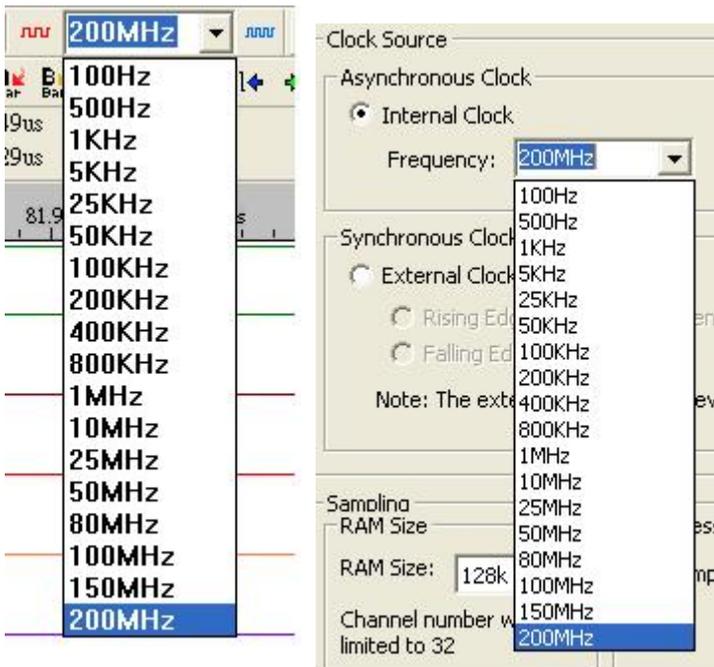


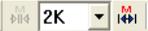
Fig 4-2 – Clock source drop down menu

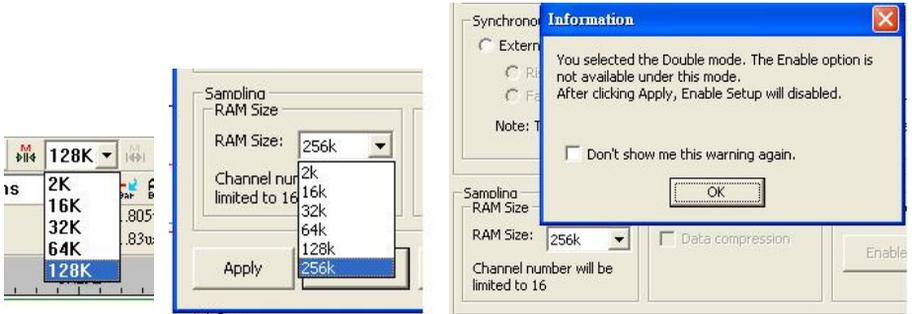
External Clock (Synchronous Clock)

Click on External Clock, and then select “Rising Edge” or “Falling Edge” as the trigger condition of the tested circuit. In the Frequency column, type the frequency of the oscillator on the tested board.

Tip: The External Clock is applied when the frequency of the oscillator on the tested board is less then 100MHz. Connect the output pin of oscillator on the tested board to the CLK pin of Logic Analyzer as shown in Fig 4-3.

Step 3. RAM size

Click on the RAM size  from the pull down menu on the Sampling Setup dialogue as shown in Fig 4-3.


Fig 4-3 – RAM Size

Tip: The relationship between RAM size and Enable and Compression and channels as shown in Table 4-1 and Fig 4-3.

Table 4-1 RAM size vs Enable, and RAM size vs Compression and channels

Model No.	RAM sizes/ channel	Channels available	Compression Mode & Enable Mode	RAM size/ channel	Channels available	Compression Mode & Enable Mode
LAP-16128U	2K ~ 128K	16 channels	Available	256K	16 channels	Disable
LAP-32128U-A	2K ~ 128K	32 channels	Available	256K	16 channels	Disable
LAP-321000U-A	2K ~ 1M	32 channels	Available	2M	16 channels	Disable

Task 2. Trigger Properties Setup

Step 1. Click  icon or Click Properties from the Trigger on the Menu Bar. The dialogue will appear as shown in Fig 4-4.

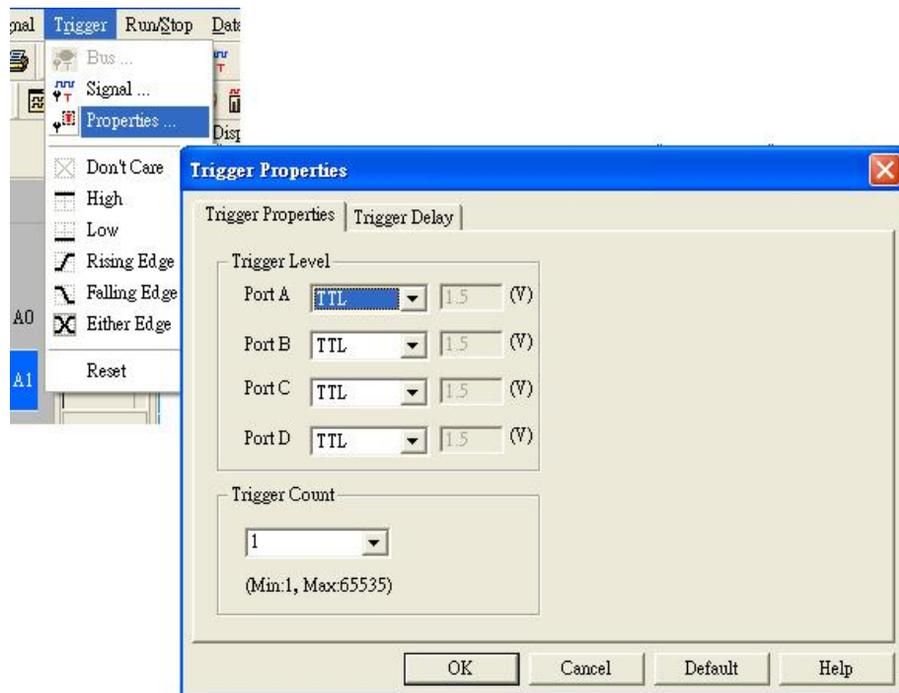


Fig 4-4 – Trigger Properties

Step 2. Trigger Level Setup

Click the drop down menu of Trigger Level on Ports A , B , C and D to select the Trigger Level as the voltage level that a trigger source signal must reach before the trigger circuit initiates a sweep.

Tip: There are four commonly used preset voltages for Trigger Level, TTL, CMOS (5V), CMOS (3.3V), and ECL. Users also may define their own voltage from -6V to +6V to fit with their test board.

Port A represents the pins from A0 ~ A7 on the signal connector of the Logic Analyzer, and so do Ports B, C and D. The voltage of each port may be configured independently.

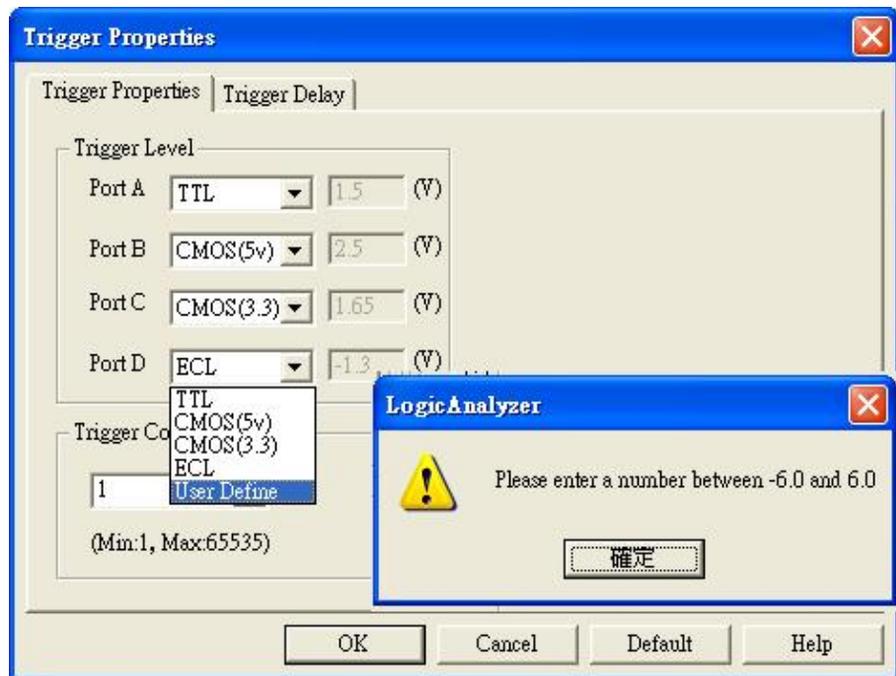


Fig 4-5 – Trigger Properties Error

Step 3. Trigger Count.

Type the numbers or select the number from the pull down menu of the Count on the Tool Bar or Click the pull down menu of the Trigger Count on the Trigger Properties dialogue as shown in Fig 4-5

The system will be triggered where the Trigger Count is set as shown in Figs 4-6,4-7 and Fig 4-8.

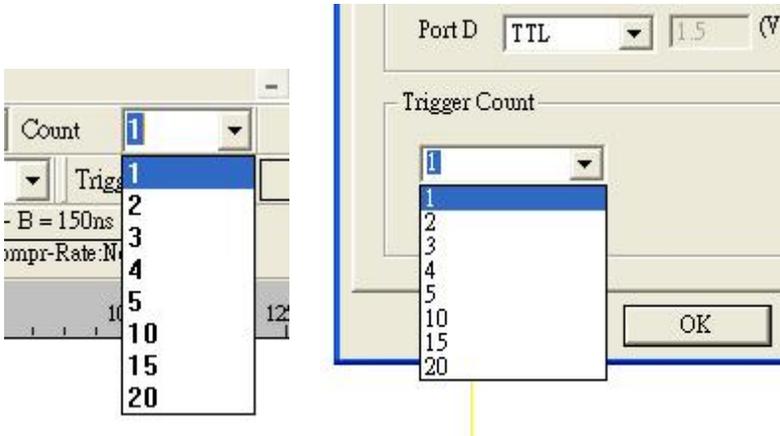


Fig 4-6 – Trigger Count Drop down Menu

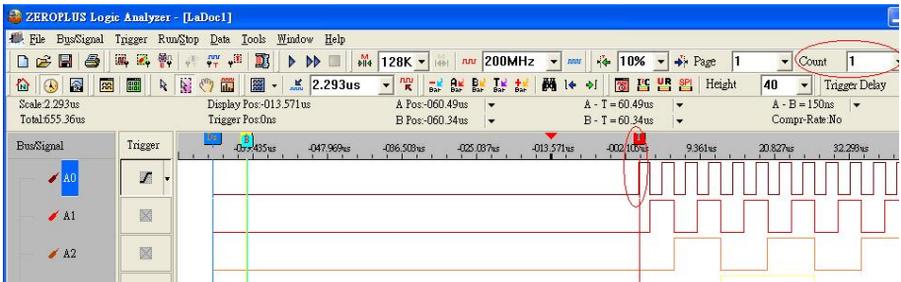


Fig 4-7 – Trigger Count Screen shot 1

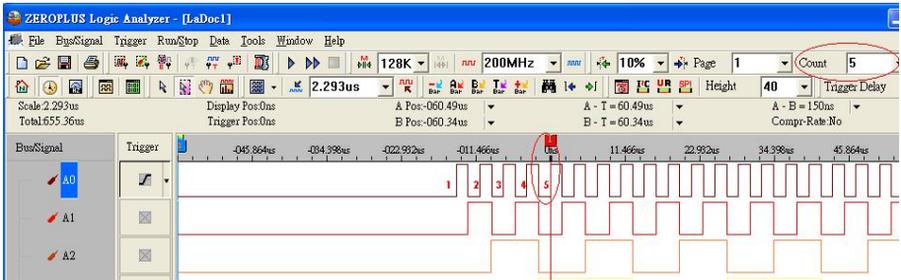


Fig 4-8 – Trigger Count Screen shot 2

Step 4. Trigger Page/ Delay Time and Clock

The Trigger Page and The Delay Time and Clock can't be applied at the same time.

1. Trigger Page:

Click Trigger Page, then Type the numbers or select the numbers from the pull down menu of the Page on the Tool Bar or Click the pull down menu of the Trigger Page on the “Trigger Delay” page of the Trigger Properties dialogue as shown in Figs 4-9,4-10 and 4-11. The page numbers selected will be displayed on the screen.

Tip: The Trigger bar (T bar) will not be displayed when the set up of the Trigger page is more than 1.

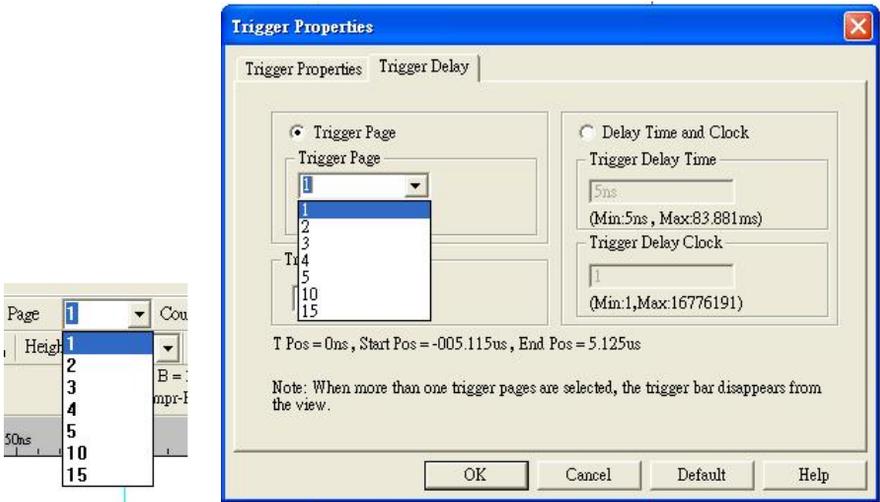


Fig 4-9 – Trigger Page

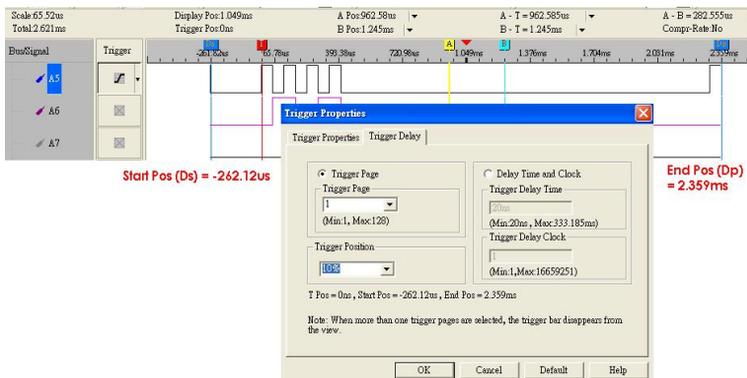


Fig 4-10 – Trigger Position

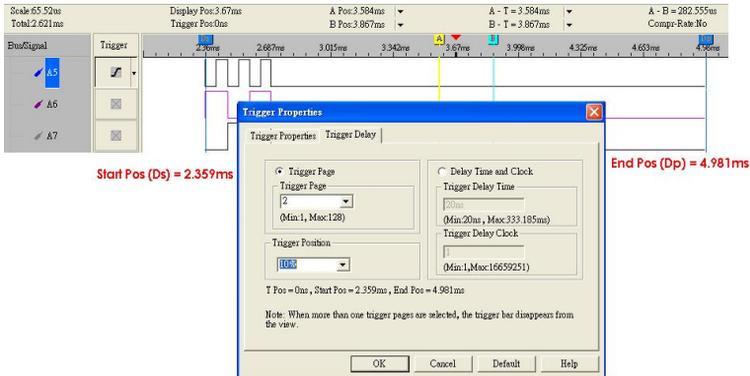


Fig 4-11 – Trigger Position and screen

2. Delay Time and Clock

Click the Delay Time and Clock, then type the numbers into the column of the Trigger Delay Time or type numbers into the Trigger Delay Clock at the “Trigger Delay” page of the Trigger Properties dialogue as 0 and Fig 0. Or type the numbers into the column of Trigger Delay on the Tool Bar. The system will display the wave start.

Tip: The formula of Delay Time and Clock is “Trigger Delay Time = Trigger Delay Clock * (1/ Frequency)”.

Step 5. Type the percentages or select the percentages from the pull down menu of the on the Tool Bar or Click the pull down menu of the Trigger Position on the “Trigger Delay” page of the Trigger Properties dialogue as shown in Figs 4-12, 4-13, 4-14, and 4-15, The Trigger Position percentages selected will be displayed where counted from the right side of the screen of the system.

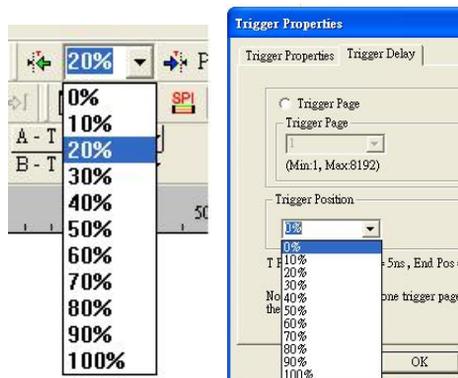
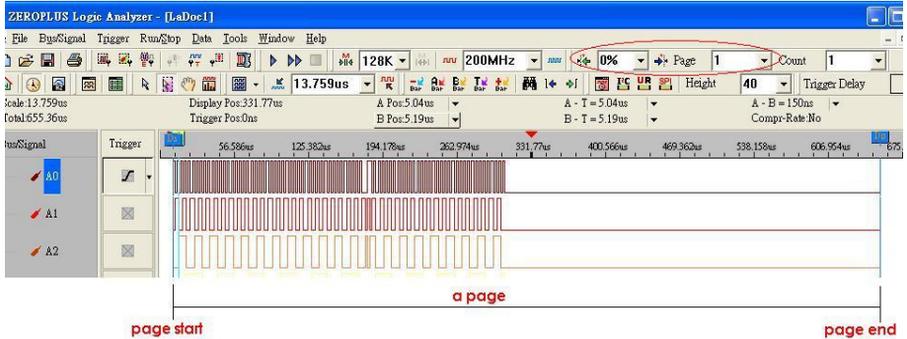
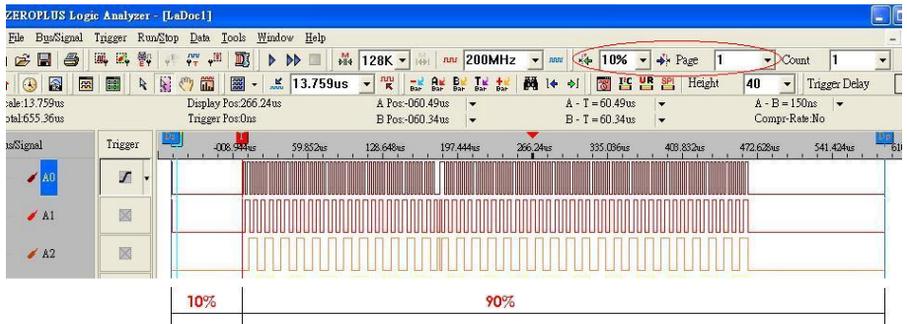
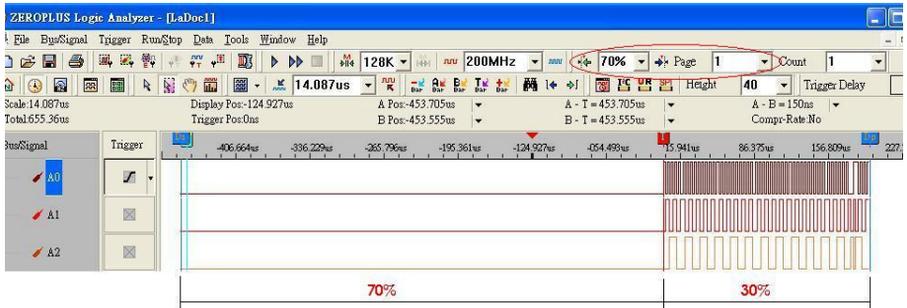


Fig 4-12 – Trigger Position Drop down menu


Fig 4-13 – Trigger Position 0%

Fig 4-14 – Trigger Position 10%

Fig 4-15 – Trigger Position 70%

Step 6. Click OK to confirm the setup and exit the dialogue of the Trigger Properties.

Task 3. Signal/Bus Trigger Edge Setup

Highlight a designated signal, and then set its required trigger edge.

1. Left click  to set the signal trigger edge as shown in Fig 4-16.
2. Right click  to set the signal trigger edge as shown in Fig 4-17.
3. Click Trigger on the menu bar and choose a trigger from the list of triggers as shown in Fig 4-18.

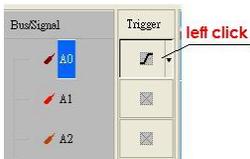


Fig 4-16 – Trigger Left click

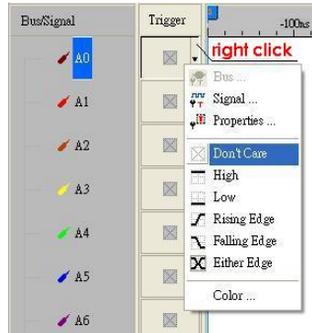


Fig 4-17 – Trigger Right Click

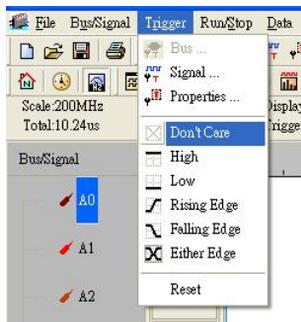


Fig 4-18 – Trigger menu

Task 4. Run to Acquire Data

1. Single Run

Click the Single Run  icon from the tool bar or press START button on top of Logic Analyzer or press F5, then activate the signal from the tested board to the Logic Analyzer to acquire the data shown in the wave display area.

2. Repetitive Run

Click the Repetitive Run  icon from the tool bar, then activate continuous signal to the Logic Analyzer to acquire the repetitive Data, and then click the

stop  icon to end the repetitive run.

Tip: Click  icon to view all the data, and then select the wave analysis tools to analyze the waves.

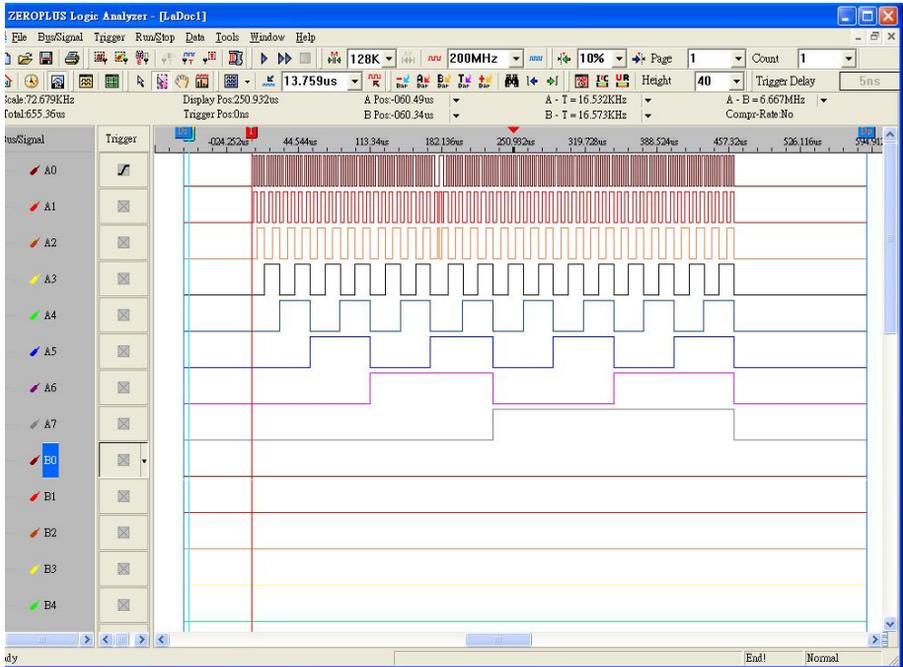


Fig 4-19 –Click  icon to view all the data

3. Stop to End Run

Click the Stop  icon to End the Run.

Tip: If the status stays displays “Waiting...” with no signal output as shown in Fig 4-20, click the stop  icon to end the run, check the setup again, and try the run process again.

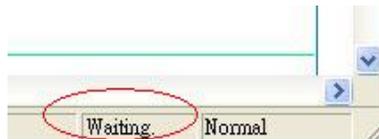


Fig 4-20 – Waiting Status

4.2 The Bus Logic Analysis

Section 4.2 presents detailed instructions about logic analysis with a set of grouped signals, which is known as the Bus Logic Analysis.

Basic Software setup of the Bus Logic Analysis

Step 1. Set up the RAM size, Frequency, Trigger level and Trigger position as descibed in Section 4.1.

Step 2. Group Signals into a Bus

Click Channels setup on Bus/Signal of menu bar, or click icon. The dialogue window shown in Fig 4-21 will appear.

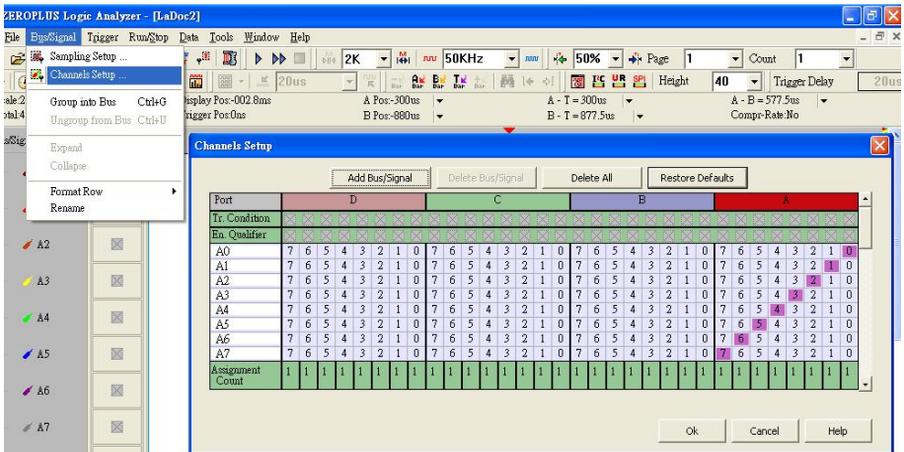


Fig 4-21 – Channel setup

Rename the bus and set up the signals of the bus as shown in Fig 4-22.

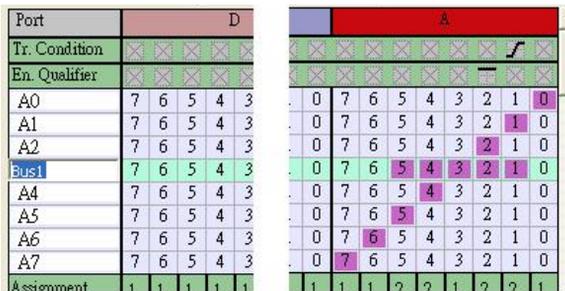


Fig 4-22 – Renaming Bus

1. Click the column with blue, then type the given name of the bus, and then press enter to confirm it.
2. Go to the relative channels show as shown in the example and, go to numbers 1,2,3,4,5 which are located on column A and row Bus1. Click them, to become purple, to set these segments of signals.
3. Click OK to get the result as shown in 0 area 1.

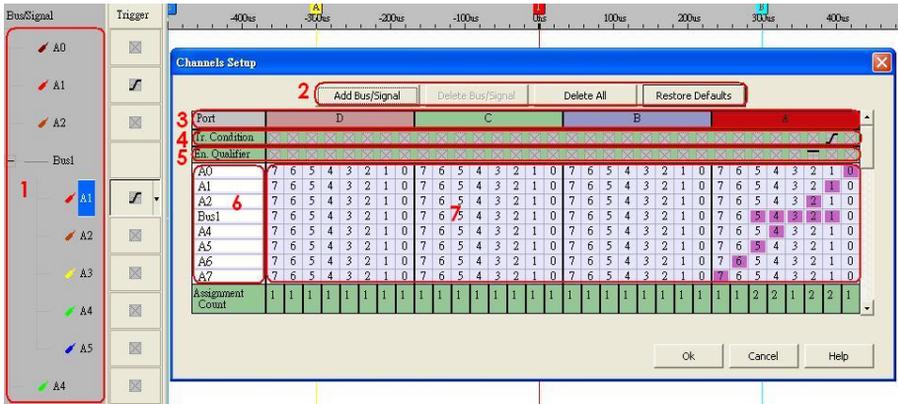


Fig 4-23 – Channel setup Window

Tip: Channels Setup

In Dialogue of Channels Setup, there isn't only Add Bus/Signal, but also Delete Bus/Signal, Delete All, Restore Defaults functions provided.

1. Delete Bus/Signal, first highlight the bus or channels on area 6 of Fig 4-23, then click Delete Bus/Signal to delete it.
2. Delete All, click Delete All to delete all bus/signals on area 6 of Fig 4-23.
3. Restore Defaults, click Restore Defaults to restore the dialogue of Channels Setup as shown in Fig 4-21.

Step 3. Set Trigger condition

1. Highlight the bus which will be triggered then click  icon or select Bus from the Trigger of the Menu bar, the dialogue window as shown in Fig 4-24 will appear.



Fig 4-24 – Bus Trigger Setup

Tip: or double click on trigger column of the bus as shown in Fig 4-25.

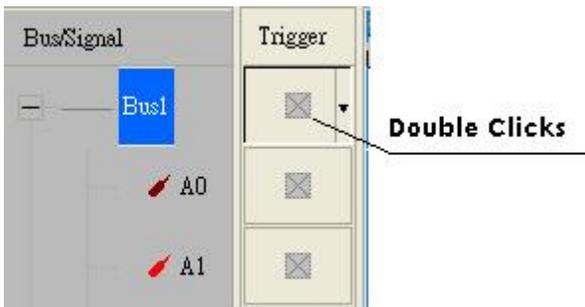


Fig 4-25 – Trigger Column

2. Set Binary, Hexadecimal or Decimal as the signal of the bus to represent the value(see Fig 4-24).
3. Set “= =” and type the value of bus into value column to set the trigger condition of the bus.
4. Click OK,

Step 4. Click run and activate the signal from the tested board to the system to get the result as shown in Fig 4-26.

Tip: Click  icon to view all data, and then select the wave analysis tools to analyze the waves.

Set Value is 5E as Hexadecimal, and set Operator equal to “= =”, then click OK, Click run and activate the signal from the tested board to the system to get the result as the trigger happens on 0X5E.

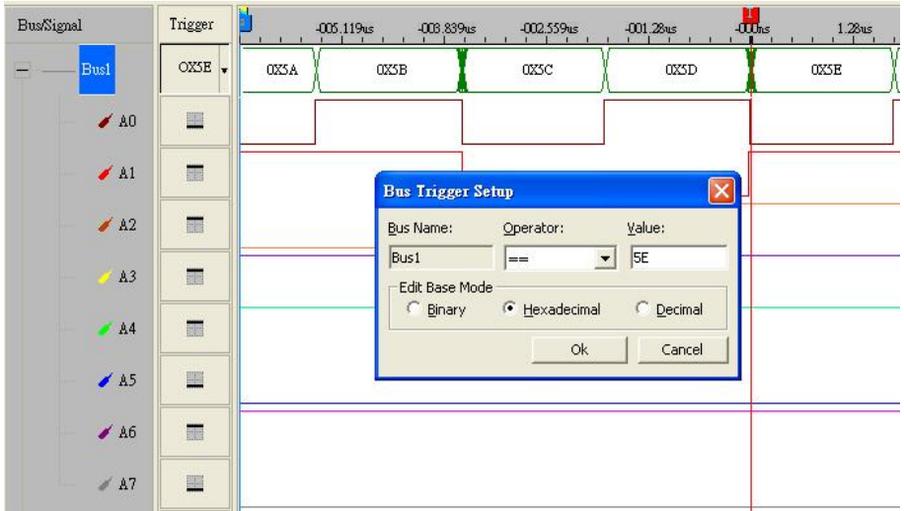


Fig 4-26 – Bus Trigger Setup

4.3 The IIC Analysis

Introduction to IIC

The IIC, which stands for Inter-Integrated Circuits, is a serial synchronous half-duplex communication protocol. The IIC is first proposed by Philips Semiconductor Nederland. This IIC protocol consists of a very simple physical interface which has only two signal wires: SDA (Serial Data Line) and SCK (Serial Clock Line). Most IIC devices consist of an independently sealed IIC chip, and this IIC chip has direct connection to both SDA and SCK. The data transmission is a byte-base (8-bit base) for every segment. Since common seen oscilloscopes do not allow engineers observe timing sequence information direction from the screens of oscilloscopes, then develop this Logic Analyzer to help engineers resolve timing sequence issues during their circuit development. There are two thing needed to be understood before performing any related tasks.

IIC has a multi-control bus as its physical and firmware interfaces. This bus is basically a signal network that may connect to single or multi control unit. The intention of inventing this protocol is in the application of designing television sets, which allows the central processing/controlling unit having fast data communications with peripheral chips and devices. This IIC interface is initiated with a SDA triggered **High** and SCK triggered **Falling Edge**. Following the initiation, there will be a set of 7 bits or 10 bits address space. Beyond this point, there will be then Read/Write, ACK (Acknowledgement), and STOP (or HALT/HLT). The signal information package is transmitted in the unit of bytes. If there are two or more devices trying to access the IIC protocol, whichever the one that have SCK at high voltage will gain the access priority.

Furthermore, since IIC is a synchronous communication protocol and data transmission must be in bytes, a complete IIC signal package must consists of **START**, **ADDRESS**, **READ/WRITE**, **DATA**, **ACK**, and **STOP** segments. They are as following.

- START:** This is the initiation of SCL and SDA which costs 1 bit only.
- ADDRESS:** this identifies the device address which costs 7 bit.
- READ/WRITE:** This is a data direction bit. 0 = Write, 1 = Read.
- ACK/NACK:** This is a confirmation bit following every data transmission segment.
- DATA:** The actual signal data transmitted by byte.
- STOP:** This is when SCL = High and SDA = Low which costs 1bit.

4.3.1 The Software Basic Setup of IIC Analysis

- Step 1.** Set up RAM size, Frequency, Trigger level and Trigger position as described in Section 4.1.
- Step 2.** Set up the falling edge of the trigger condition on the signal which connects to the tested IIC data pin (SDA).
- Step 3.** Click  icon or select the Analyze IIC wave on the Tools of the manual bar. The dialogue of the special Bus IIC setup (Fig 4-27) will appear.

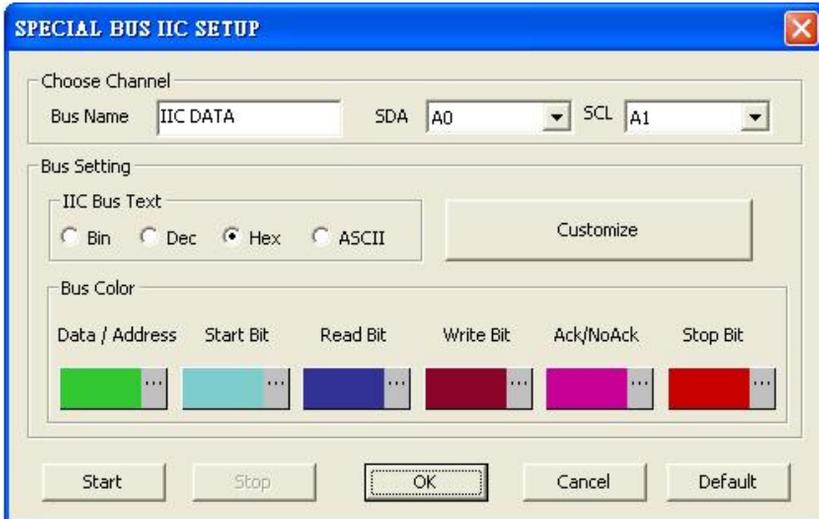


Fig 4-27 – Special Bus IIC Setup

Step 4.

1. Bus Name: Set the display name of IIC in Data Bus.
2. SDA: Choose SDA channel of IIC
3. SCL: Choose SCL channels of IIC

Note: It is recommended that SDA and SCL channels are named SDA and SCL to help distinguish between them.

4. IIC Bus Text: Choose the display word of IIC in the Data Bus, including Binary, the Decimal and ASCII.
5. Bus Color: set the segment of colors in Data Bus to that the segment, the initial unit, reading unit, writing unit, confirmation unit and the end unit will be embedded in the Data Bus.

Step 5. Click IIC Customize to define the IIC Data Bus to meet user's requirement. The dialogue as shown in Fig 4-28 will be displayed.

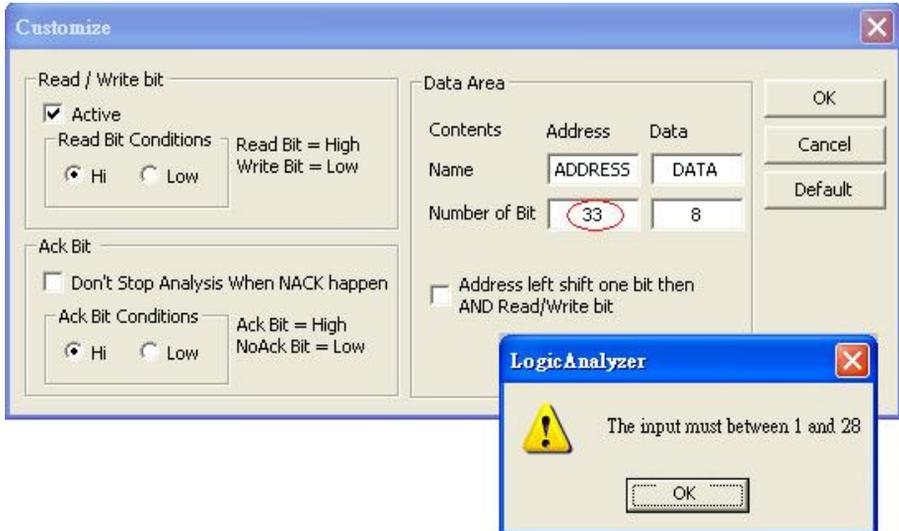


Fig 4-28 – Inputting Data Bits

1. Read/ Write Setup:

Click on “Active” to set the segment of Read/ Write bit in the IIC Data Bus, then select “High” or “Low” to set the active condition of the Read/ Write bit for the tested board.

Click off Active to remove the Read/ Write bit segment from the IIC Data Bus

2. Ack bit set up:

Click on “Don’t Stop Analysis when NACK happen” to continuously analyze the signals when the system says NACK bit, then select “High” or “Low” to set the active condition of the NACK bit for the tested IIC bus.

Click off “Don’t Stop Analysis when NACK happen” to stop analyze of the signals when the system reads NACK bit.

3. Give the names and the numbers of bits to the Address bit and Data bit on the columns located in Data area for the tested IIC bus.

The range for Bit set up is from 1 to 28 bits.

4. Click on “Address left shift one bit then AND Read/Write bit” to have an additional 1 bit on the right side of the Address Data content.

5. Press OK to confirm the set up of IIC customize and return to Special Bus IIC Setup dialogue. (Tip: Press Default to give up the current Setup conditions)

Step 6. Click Start, then Press OK from the dialogue of Special Bus IIC Setup.

Step 7. Click Run, then Active IIC signal to acquire the result on the bottom of wave display area.

Tip: Click the IIC icon, then press Stop to exit IIC analyze mode.

Tip: Click  icon to view all data, and then select the wave analyze tools to analyze the waves.

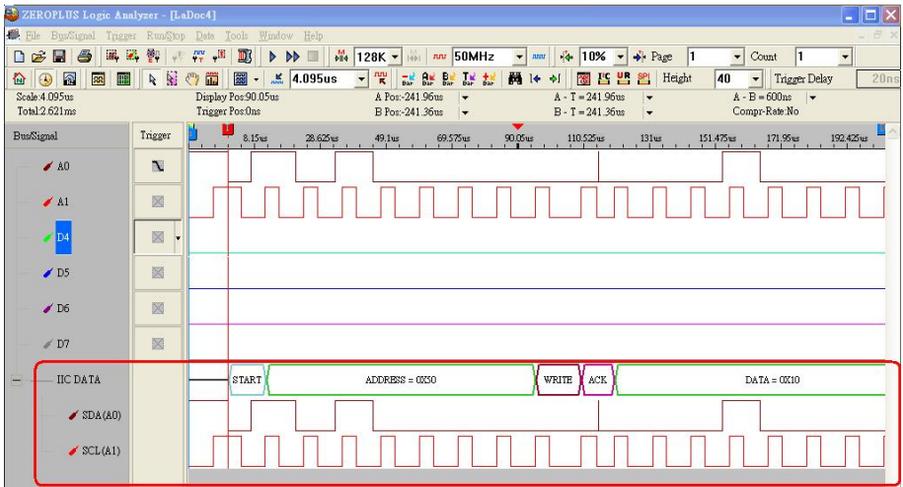


Fig 4-29 – Wave analysis

4.4 UART Analysis

Introduction to UART

The UART, which stands for Universal Asynchronous Receiver/Transmitter, is a serial asynchronous protocol. The physical interface require only on wire. The UART is often time integrated into PC communication devices, and it usually equips an EEPROM (Electronic Erasable/Programmable Read Only Memory.) for error checking proposes with other chips. There are two ideas about UART which must be understood before performing any further task.

The UART protocol will first translate a parallel data in to serial data, for the UART require only on wire to transmit signals. The transmission starts at a triggered Low position, and there are 7 or 8 bit of data following afterwards. To halt a transmission, it requires a signal or multiple bits of **High** bit. Odd number bit transmission requires odd parity error checking, and even umber bit transmission requires even number error checking. Following the parity checking is another data translation from serial data into parallel data. UART also generates extra signal to indicate receiving and transmitting conditions.

Furthermore, since UART is an asynchronous communication protocol and data transmission may not be in bytes, a complete UART signal package must consists of **START**, **DATA**, **Parity check**, **STOP**, **Buad**, and **TXD** segments. They are as following :

- START:** When TXD is changing form **HIGH** to **LOW** voltage. This costs 1 bit..
- DATA:** Users must decide the size of signal package segment from 4 to 8bits.
- Parity Check:** This performs three types of parity checks: odd-parity, even-parity, and none-parity.
- STOP:** This occurs when TXD is at high voltage. This is adjustable; this is commonly set to 1 or 2.
- Baud:** This is the data transmission speed according to the START initial condition.
- TXD:** This is the transmission direction. It is LSM → MSB by default.

4.4.1 The Software Basic Setup of UART

- Step 1.** Set up RAM size, Frequency, Trigger level and Trigger position as described in Section 4.1. (Tip: The Setup of the Frequency should be higher then but not to far away from the Baud Rate of the tested board).
- Step 2.** Set up either edge  as the trigger condition on the signals which are connected to the Tx pin or the Rx pin of the tested UART board.
- Step 3.** Click  icon or select the Analyze UART wave on the Tools of the menumenu bar. The dialogue of the special Bus UART setup shown in Fig 4-30 will appear.

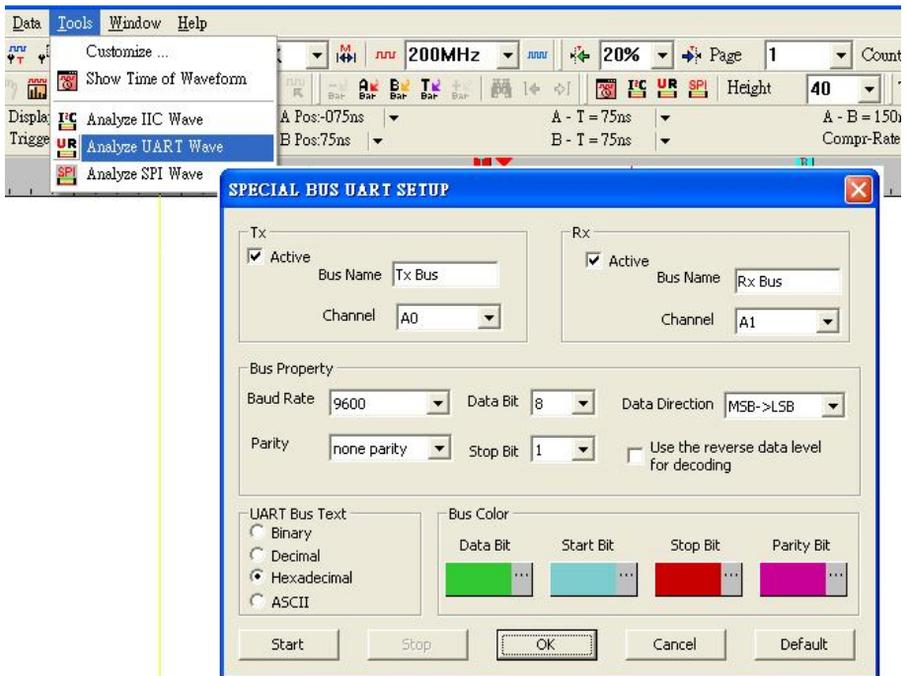


Fig 4-30 – UART Setup

Step 4. Special Bus UART Setup

1. Set the Data of the Transmitter Signal.

Click on “Active” of Tx, then type the given Bus name on column of Bus Name, then select the signal which is connected to the Tx pin of the tested board from the pull down menumenu to analyze the data of the transmitter signal.

2. Set the Data of the Receiver Signal.

Click on “Active” of Rx, then type given Bus name on column of Bus Name, then select the signal which connected to the Rx pin of the tested board from the pull down menu to analyze the data of the receiver signal.

3. Set the Baud Rate.

Select the rate from the pull down menu of the Baud Rate to meet the specification of the tested UART board. Baud Rate may be set equal to 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600 or 115200.

4. Set the Bits of the Data Bit.

Select the number from the pull down menu of the Data Bit to meet the specification of the tested UART board. Data Bits may be set to 4, 5, 6, 7 or 8.

5. Set the Data Direction.

Select MSB => LSB or LSB => MSB from the pull down menu of the Data Direction to meet the specification of the tested UART board.

Tip: Select MSB => LSB to arrange data from left to right eg. 0-0-0-1=0001; Select LSB => MSB to arrange data from right to left eg. 1-0-0-0=0001 as Fig 4-31.



Fig 4-31 – Data waves MSB=>LSB and LSB=>MSB

6. Set the Parity

Select none parity, odd parity or even parity from the pull down menu of Parity Setup to meet the specification of the tested UART board. (Tip: “Error-1” will be indicated on the parity bit of the UART wave when the data contents of the tested UART board don’t meet the Setup of the Parity Setup.)

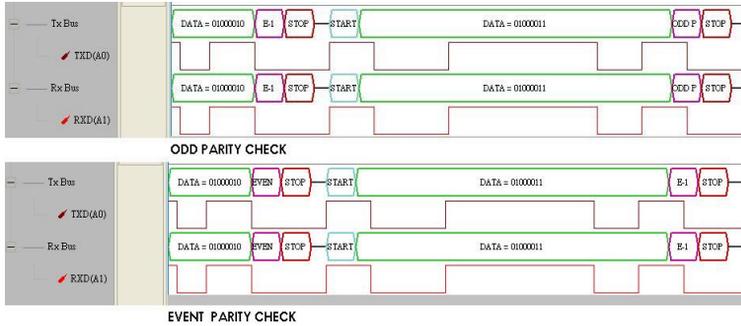


Fig 4-32 – Odd and Even Parity Check

7. Set the Bits of the Stop Bit.

Select the number from the pull down menu of the Stop Bit to meet the specification of the tested UART board. Stop Bit may be set to 1, 1.5 or 2.

8. Set “Use the reverse data level for decoding”.

Click on “Use the reverse data level for decoding” to decode the data received into the negative logic which a negative voltage represents the 1 state and a positive voltage represents the 0 state.

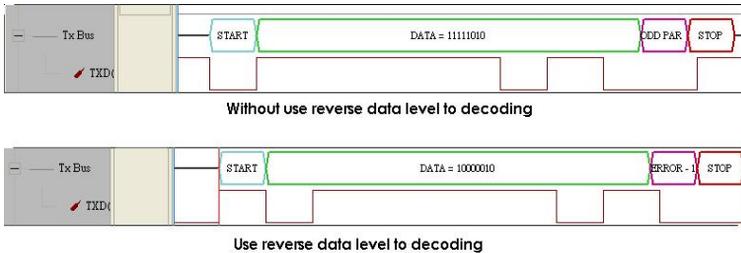


Fig 4-33 – Without/With data level decoding

9. Set Bus Color

Click the color of the bus segment as the data bit, the start bit, the stop bit, the parity bit to select the required color.

Step 5. Click Start, then Press OK from the dialogue of Special Bus UART Setup.

Step 6. Click Run, then Active the UART signal from the tested UART circuit to acquire the result on the bottom of the wave display area as shown in Fig 4-34.

Tip: Click the UART icon, then press Stop to exit the UART analysis mode.

Tip: Click  icon to view all data, and then select the wave analysis tools to analyze the waves.

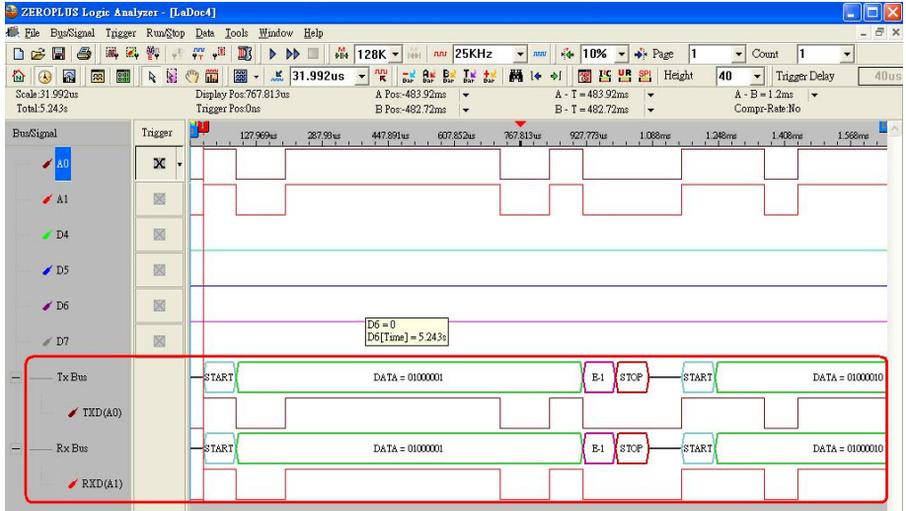


Fig 4-34 – Wave Analysis

4.5 The SPI Analysis

Introduction to SPI

The SPI, (Synchronous Peripheral Interface), is a parallel synchronous full duplex protocol with a bus-like physical interface. This protocol was first developed by Motorola and was generally used for EEPROM, ADC, FRAM, and display device drivers which are devices with low data transmission speeds. The SPI data transmission is synchronous in both receiving and transmitting directions. Although Motorola initially does not define the clocking impulse, it is commonly seen that the clocking impulse is according to the master processor. In practice, there are two clocking impulses: CPOL (Clock Polarity) and CPHA (Clock Phase). The configuration of both CPOC and CPHA decides the sampling rate. When the SPI must transmit a serial data, it initiates the highest bit.

Since SPI is a synchronous communication protocol and data transmission may not be in bytes, a complete SPI signal package must consist of SCK, MOSI, MISO, and SS segments with CPHA and CPOL. They are as following.

SCK: Serial Clock Line, a.k.a. SCL.

MOSI: Master data output, Slave data input (MOSI stands for Master-Out-Slave-In)

MISO: Master data input, Slave data output (MISO stands for Master-In-Slave-Out)

SS: SS stands for Signal Selector of the master device which is to select signals for the Slave devices.

CPHA: the clock phase (CPHA) control bit selects one of the two fundamentally different transfer formats.

CPOL: the clock polarity is specified by the CPOL control bit, which selects an active high or active low clock.

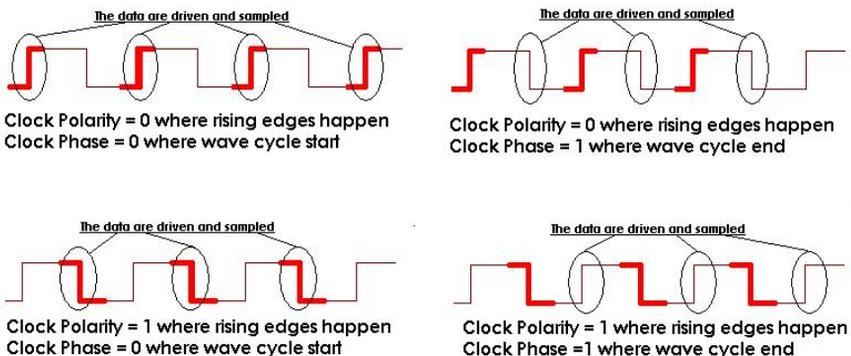


Fig 4-35 – Clock Polarity and Phases

4.5.1 The Software Basic Setup of SPI

- Step 1.** Set up RAM size, Frequency, Trigger level and Trigger position as described in Section 4.1.
- Step 2.** Set up the falling edge on the signal of SS which connected to the Signal Selector (SS) pin of the SPI tested board.
- Step 3.** Click  icon or select the Analyze SPI wave on the Tools of the menu bar. The dialogue of the Bus SPI setting will appear (see Fig 4-36).

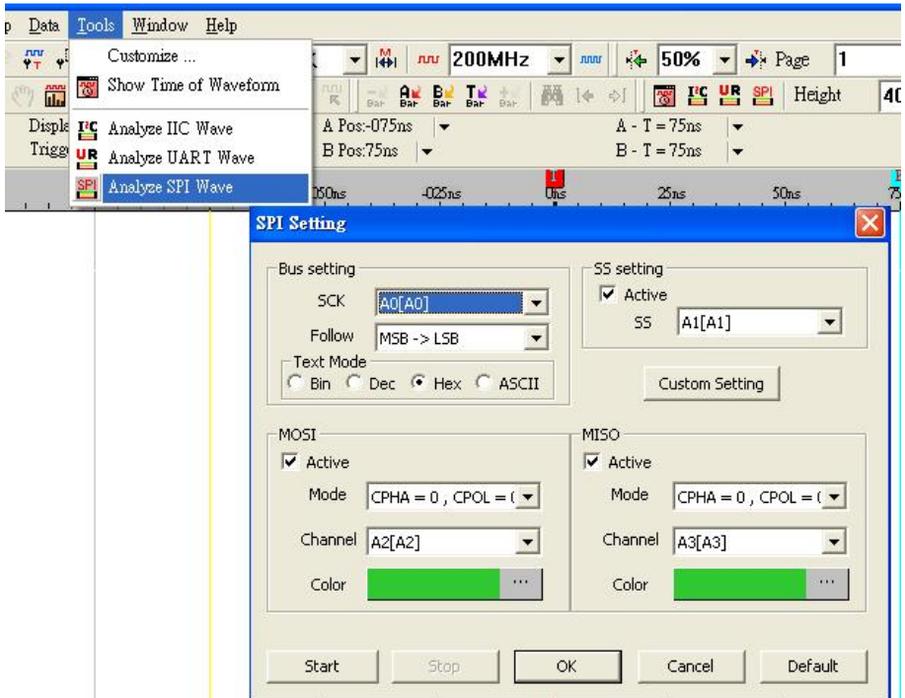


Fig 4-36 – Analyze SPI Wave

Step 4. SPI Setup

1. SCK Bus Setting

Select the Signal which connects to the Serial Clock pin of the tested SPI board from pull down menu of “SCK”.

Then Select MSB => LSB or LSB => MSB from the pull down menu of the “Follow” to meet the specifications of the tested SPI circuit.

Then select the test as Bin (Binary),e Dec (Decimal),Hex (Hexadecimal) or ASCII to present the contents of the Bus.

Tip: Select MSB => LSB to arrange data from left to right eg. 0-0-0-1=0001;
Select LSB => MSB to arrange data from right to left eg. 1-0-0-0=0001

2. MOSI Setting

Click Active to on MOSI (Master-Out-Slave-In).

Then select the CPOL (Clock polarity) and the CPHA (Clock Phase) from the pull down menu of the "Mode" to meet the specifications of the tested SPI circuit.

Then select the Signal which connects to the Master-Out-Slave-In pin of the tested SPI board from pull down menu of "Channel".

Then click color and select a color to define the MOSI signal.

3. MISO Setting

Click Active to on MISO (Master-In-Slave-Out).

Then select the CPOL (Clock polarity) and the CPHA (Clock Phase) from the pull down menu of the "Mode" to meet the specification of the tested SPI circuit.

Then select the Signal connected to the Master-In-Slave-Out pin of the tested SPI board from pull down menu of "Channel".

Then click color and select a color to define the MISO signal.

4. SS Setting

Click Active to on SS (Signal Selector).

Then select the Signal which connects to the Signal Selector pin of the tested SPI board from pull down menu of "SS".

5. Custom Setting

A. SS Setting is Active

Click the Custom Setting, the dialogue of the SPI Custom Setting will appear as shown in Fig 4-37.

(1) Select "High" or "Low" to define the SS enable level of the tested SPI circuit.

(2) Then type the name and the numbers of the data bit for the MOSI signal.

(3) Press OK to confirm the set up of SPI custom Setting and return to the dialogue of the SPI Setting. (Tip: Press Default to give up the current Setup conditions)

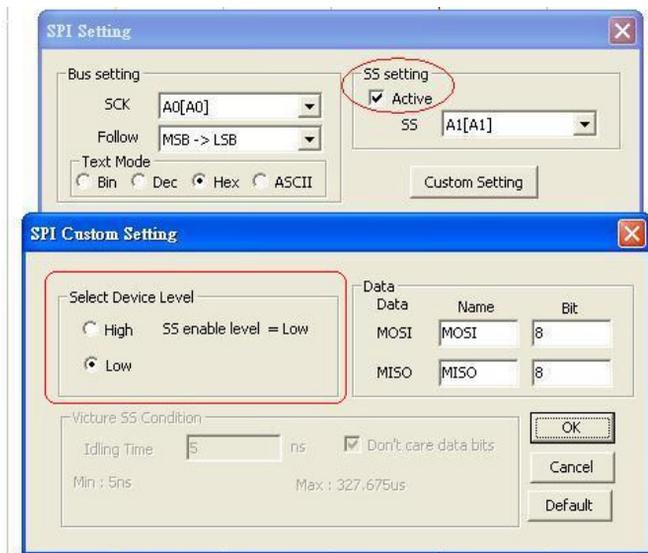


Fig 4-37 – SPI Custom Setting

B. SS Setting is not Active

Click the Custom Setting, in the dialogue of the SPI Custom Setting will appear as shown in Fig 4-38.

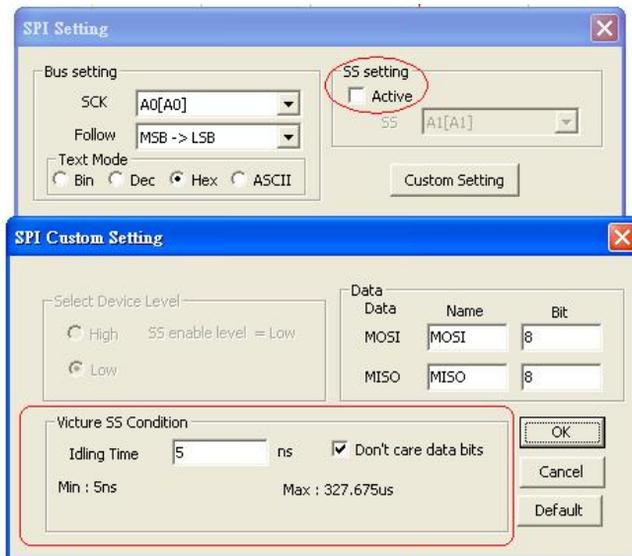


Fig 4-38 – Victure SS Condition

(4)Type the idling time of the SCK signal on the tested SPI circuit. The

idling time is defined as the idling time as shown in Fig 4-39.

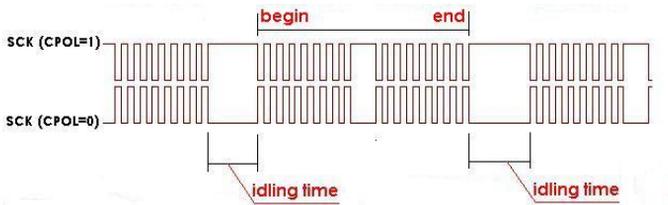


Fig 4-39 – Idling time

- (5) Click on the “Don’t care data bits” function. The system will restart and count from the beginning of the data bits when the condition of the idling time set is qualified.
- (6) Click off the “Don’t care data bits” function, the system will decode the data stilly until the bits of the data are received completely, when the condition of the idling time set is qualified.
- (7) Then type the name and the numbers of the data bit for the MOSI signal.
- (8) Press OK to confirm the set up of SPI custom Setting and return to the dialogue of the SPI Setting. (Tip: Press Default to give up the current Setup conditions)

Step 5. Click Start to confirm the setup of SPI setting and click OK to exit the dialogue of SPI setting.

Step 6. Click Run, then Active the SPI signal from the tested SPI circuit to acquire the result on the bottom of the wave display area as shown in Fig 4-40.

Tip: Click  icon to view all the data, and then select the wave analysis tools to analyze the waves.

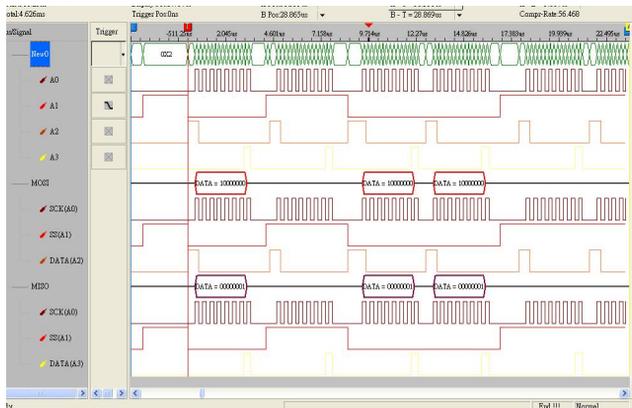


Fig 4-40 – Active SPI signal

4.6 Compression

The function of compression is to enable the system to compress the signal received and have more data stored in the memory per channel.

4.6.1 The Software Basic Setup of Compression

- Step 1.** Set up RAM size, Frequency, Trigger level and Trigger position as described in Section 4.1.
- Step 2.** Set up the trigger edge on the signal or the bus to be triggered.
- Step 3.** Click  icon, or click the compression function from the sampling setup dialogue then click Apply and OK to run.

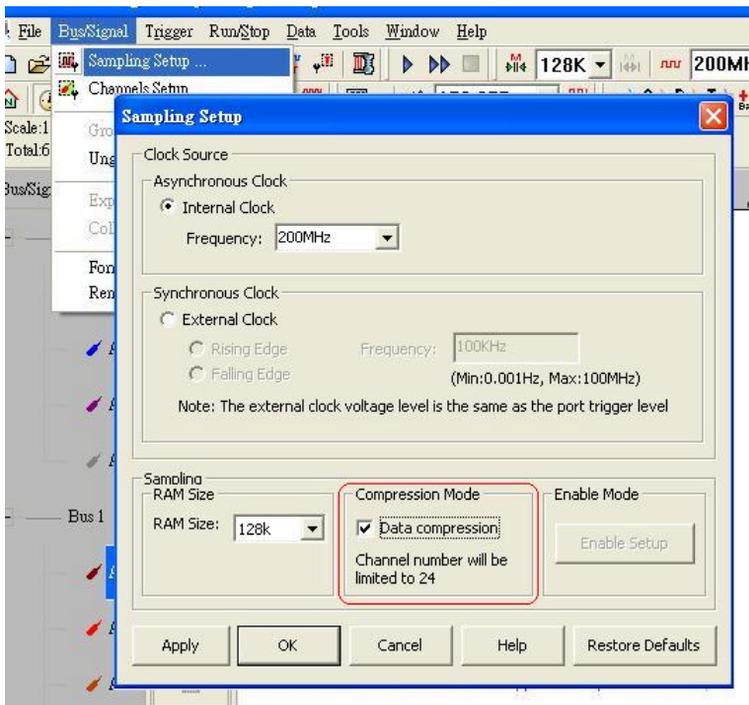


Fig 4-41 – Compression Mode

- Step 4.** Click Run, and then activate the signal from the tested circuit to acquire the result on the wave display area. Fig 4-42 show the result before and after compression has been applied.

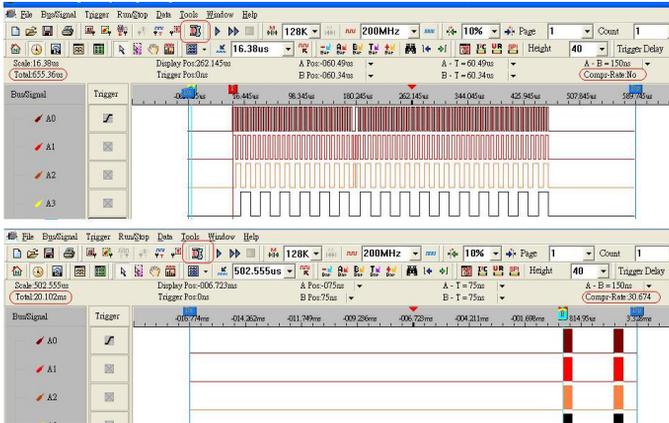


Fig 4-42 – Before and After Compression

Using 128K memory depth, before compression has been applied, the total of the data was 655.36us, after the compression had been applied, the total of the data was 20.102ms, the compression rate is 30.674.

Tip: Click  icon to view all data, then select the wave analyze tools to analyze the waves.

Step 5. Click the compression icon again or click off the compression function to stop compression.

Tip: Compression cannot be applied with the enable function at the same time.

4.7 Enable and Enable Delay

The function of the Enable and Enable Delay is to allow the system to keep the wave required, and filter out the waves that aren't required.

4.7.1 The software Basic Setup of Enable and Enable Delay

The Software Basic Setup of Enable / Enable Delay

Step 1. Set up RAM size, Frequency, Trigger level and Trigger position as described in Section 4.1.

Step 2. Set up the trigger edge on the signal or the bus to be triggered.

Step 3. Click  icon, or click the Enable function from the sampling setup dialogue and the Enable Setup dialogue will appear.

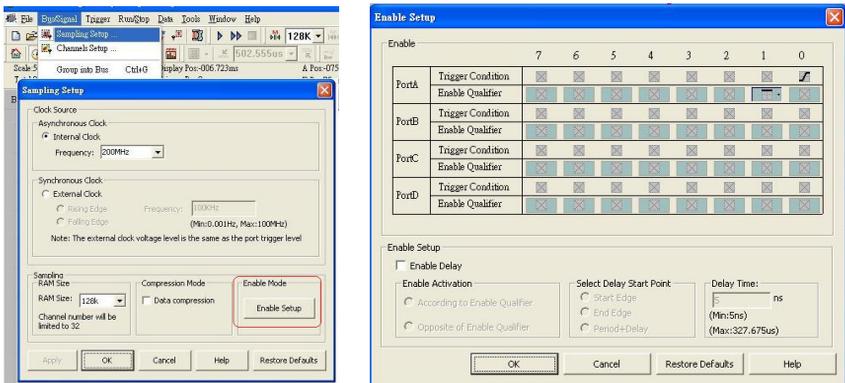


Fig 4-43 – Enable Setup

Set the high edge as Enable Qualifier on the signal A1.

Step 4. Enable

1. Setup the Enable Qualifier as  or  on the signal to be analyzed.
2. Click OK, then click run and activate the signal from the tested circuit to the Logic Analyzer.
3. The system will only display the waves of the signals which are qualified by the setup of the Enable Qualifier.

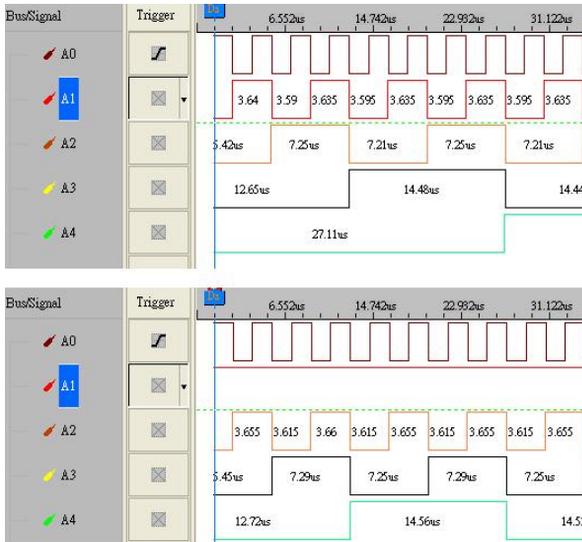


Fig 4-44 – Without/With enable setup

The first picture shows the result without any enable setup.

The second picture shows the result which has set the high edge on the enable qualifier of the signal A1. Only high status of the A1 wave is display.

Step 5. Enable Delay

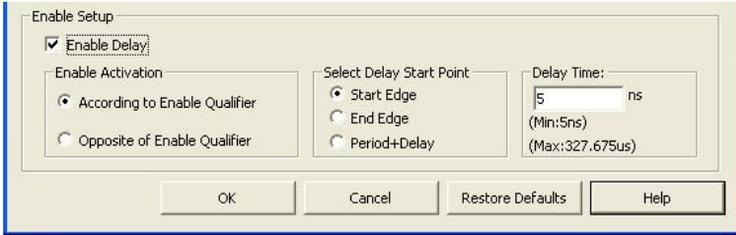
1. Click on the Enable Delay function as shown as Fig 4-45.
2. Click on the “According to Enable Qualifier or the “Opposite of Enable Qualifier” functions to select the waves to be kept.
3. Click on the “Start Edge”, “End Edge” or “Period + Delay” functions to set the Start Point of Delay.
4. Type the value of the Delay Time into the column of the Delay Time.
5. Click Ok, then click run and activate the signal from the tested circuit to the Logic Analyzer.
6. The result will be displayed in the wave display area as shown in Fig 4-44.

Step 6. Stop Enable/ Enable Delay

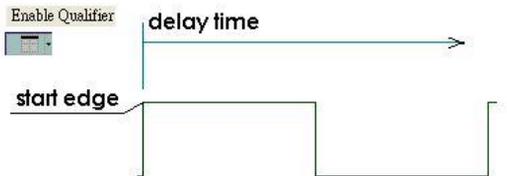
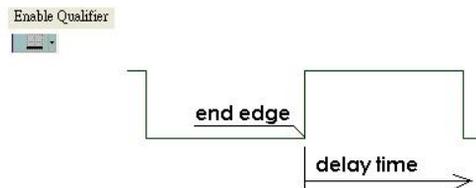
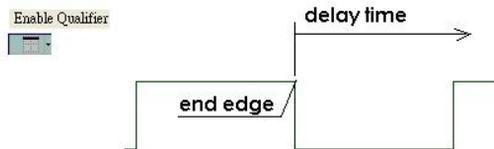
Click Stop, then click enable icon and select cancel from the Enable Setup dialogue to stop the enable or the enable delay functions.

Tip: Run the Stop Enable function to check the conditions of the enable or the enable delay setup, if there aren't any results.

Tip: Click  icon to view all the data, and then select the wave analysis tools to analyze the waves.


Fig 4-45 – Enable Delay

Tip: Definitions of the Start Edge and the End Edge and the Period + Delay are listed as Figs 4-46, 4-47, 4-48 and 4-49.


Fig 4-46 – Start Edge

Fig 4-47 – End Edge

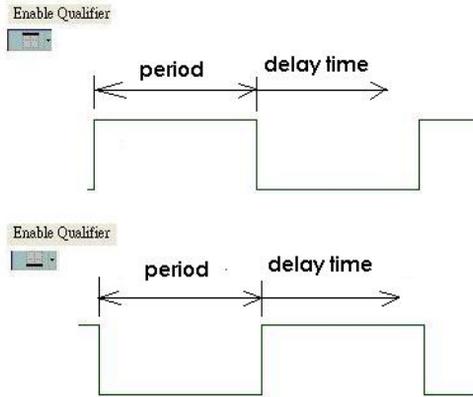


Fig 4-48 – Period and Delay Time

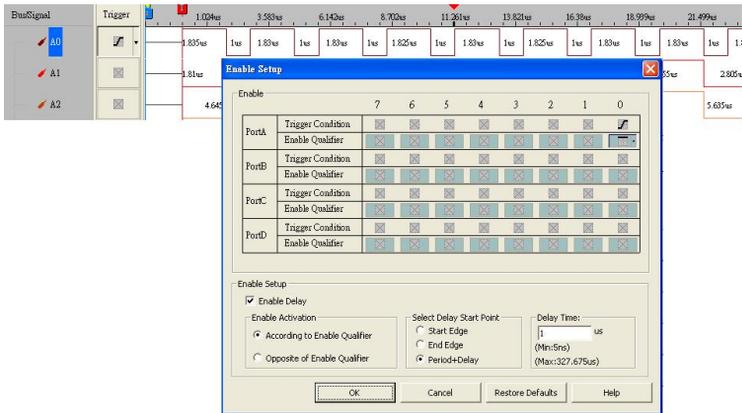


Fig 4-49 – Enable Delay Setup

Signal A0 has got 1 us delay time as the condition of the Enable Delay setup.

5 Troubleshooting

- 5.1 Installation Troubleshooting
- 5.2 Software Troubleshooting
- 5.3 Hardware Troubleshooting

Objective

In this chapter, troubleshooting is classified into installation, software and hardware. These troubleshooting questions and answers depend not only on our engineers, but also on end users such as students, engineers, technical manual writers, and others..

5.1 Installation Troubleshooting

Q1. Why is there no prompt when I insert the driver CD into my CD-ROM?

A: At this stage, the driver CD is not auto-executable. The primary issue here is a chipset problem. Though these three Logic Analyzer models seem only different in model number, they are quite different in firmware and chipsets. Due to installation procedures (see *Chapter 2*), we are unable to compile a driver program that auto-detects the chipset at the beginning of installation.

Q2. Why does the installation software keep giving an error message saying that I don't have enough memory?

A: This kind of problem happens in many hardware installations. Turn off multimedia programs such as Media Player, media decoders, media encoders, and so on. If there are any multimedia icons in the system tray (see the far right end of the **START** menu taskbar), remove them. The Logic Analyzer software will run better in memory locations from 64 to 512 MB.

Q3. What if I want to share this software interface with all users of my computer after installing it?

A: The shortcut is removing the software interface and then reinstalling it. By default, the program is available for all users.

Q4. My HDD is modest; which software components are absolutely necessary?

A: Choose Custom as your setup type. Next (refer to *Fig 2-11*), unselect items such as examples and tutorials. You must install at least the Main App (application).

Q5. My MS Windows system will not accept the driver; what can I do?

A: Double check that you ran the correct Setup.exe from the folder that corresponds to your hardware and MS Windows version. Visit our website for the latest updated or debugged software. If you are running this program on a virtual machine, the virtual machine may not support the amount of hardware addressing. In this case, try it with a machine that is physically running a Windows system.

5.2 Software Troubleshooting

Q1. Can I run the program even if I don't have the Logic Analyzer hardware?

A: Yes, you can. You can run the program under the demo mode. See. *Fig. 5-1*.

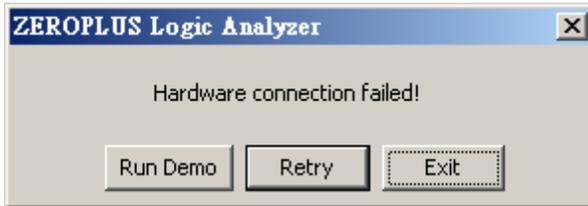


Fig. 5-1: Select **Run Demo** if you do not have the actual hardware.

Q2. I am running a graphing program and software at the same time. Whenever I try to make a screenshot of my work, it keeps telling me that I have insufficient memory space; what is wrong?

A: A few users have reported similar problems. We are not certain what causes it or how to fix it. We have found that if there is a defective address within 128 MB to 512 MB in your physical memory, your software might signal "End of memory". Thus, the program will warn you about insufficient memory. Test your memory with a varied memory testing program. Or, take a screen shot, close the program, paste it to the graphing program, and re-open the program.

Q3. A part of the background picture remains within the Position Display Area, especially when running the program in demo mode. What's wrong with it?

A: Your machine may have a memory management problem with either your physical RAM onboard or the RAM on your video card. Turn off any other multimedia of graphic programs and then re-run the software. If this does not work, restart your system. This should temporarily fix the problem. However, we highly recommend terminating all irrelevant programs while working with the Logic Analyzer (Try not to burn DVDs, listen to music or watch movies while working with the Logic Analyzer.).

Q4. The default color setting of the Position Display Area is very cool, but I don't see anything when I print my work out with my black and white laser printer. What I can I do?

A: Refer to *Section 3.4*; it should have clear, understandable instructions about changing the user interface. See *Fig. 3-93*; this color setting should give a clear view of the Position Display Area, even with an old black and white laser printer.

5.3 Hardware Troubleshooting

Q1. Why are no lights on when I hook the USB cable to the Logic Analyzer?

A: Double check whether the other end is properly connected to your PC. There may also be a defect in your USB cable. Try another cable.

Q2. Why can't I read any signals from my Logic Analyzer?

A: Check whether you have correctly connected the signal cables to the activated pin on your test board and check the power supply for your test board. The Logic Analyzer does not supply any electricity to a test board via signal lines.

Q3. I get a signal from only one Logic Analyzer when I have two connected; what is wrong?

A: Currently, only the LAP-321000U-A supports multiple Logic Analyzers working in series. Also, make sure that the signal lines, power lines, and ground line are properly connected. Refer to Fig. 1-12, Table 1-2, Table 1-3, Table 1-4, and Table 1-5.

Q4. Why bother grounding? Where can I ground?

A: Grounding will protect the Logic Analyzer and the test board. A proper ground may improve the quality and accuracy of your data. Since it is impossible to avoid unwanted interference you may ground the Logic Analyzer with the test board to ensure that unwanted interference will equally disturb both the testing and tested devices, ensuring a set of data that is still accurate.

Conclusion

Every user of a product is a potential writer for *Chapters 5~7* in this User's Manual. In fact, this chapter is a composition of many unnamed electronic professionals, especially experts.

6 FAQ

- 6.1 Hardware
- 6.2 Software
- 6.3 Registration
- 6.4 Technical information
- 6.5 Others

Objective

In this chapter, common problems and questions are roughly classified into five categories: Hardware, Software, Registration, Terminology & News, and Others. This is a backup resource for users, especially those without Internet access. Most users find this chapter very helpful. This chapter is written for non-Chinese user groups. Most references refer to English web links.

6.1 Hardware

H01. Is it ok to substitute stock items for bundled cables and connectors ?

A: Yes, users may use any compatible connectors and cables. However, to ensure consistency and accuracy in measurements and data, we strongly recommend using the bundled connectors and cables. Each of the Logic Analyzer's is calibrated with the bundled cables and connectors before packing.

H02. Does manufacture grippers? How may I purchase Grippers?

A: Yes, we have a production line dedicated to grippers. Contact our sales department and a sales representative will be happy to assist you.

H03. Is the memory size fixed? If I just use one of the ports, can I expand the memory size?

A: The Logic analyzer's memory is fixed at 4 megabits. Due to current hardware limitations, the memory size cannot be modified, even as the number of ports used changes.

H04. Are different external sampling frequencies for different channels possible?

A: No, there is only one external sample frequency available.

H05. Can I disable or set a certain port to *don't care* while during compression?

A: No, during compression, D Port will be set to be **disabled**.

H06. Why does the Logic analyzer feature negative voltage calibration?

A: This allows users to analyze any given signal.

H07. How do I adjust the Trigger Level?

A: The adjustment of the trigger level is done with a port which consists of 8 channels. The trigger lever can only be adjusted for an entire port.

H08. Does the Logic Analyzer use hardware or software compression technology?

A: For time efficiency, the Logic Analyzer uses hardware compression.

H09. Is planning an Analyzer that can handle more channels?

A: Yes, we are working in this direction.

H10. Does the memory page vary when the depth of the memory changes?

A: Yes, the depth of memory changes the memory page.

H11. Is the Logic Analyzer expandable? How may I expand it?

A: Yes, the Logic Analyzer is expandable. At this stage, you can expand it with external module devices.

H12. Why must I reinstall the driver every time I use a different the Logic Analyzer?

A: Since each the Logic Analyzer has unique serial numbers, you must reinstall the driver every time you change the Logic analyzer.

H13. Why is there no data? Why does data sampling seem inconsistent?

A: The reasons are varied, but you may follow this checklist for troubleshooting:

- 1) Always check the USB connection between the Logic analyzer and your PC.
- 2) We strongly recommend using USB ports in the rear panel of a PC; these ports usually have better voltage stabilities than front panel ports. However, if front panel USB ports are directly soldered to the main board, you can use them.
- 3) Make sure the Logic analyzer is directly connected with the PC (without a USB hub).
- 4) Inconsistent data display may indicate voltage irregularities in the main board; examine capacitors on your main board or power supply.
- 5) If the problem is the power supply, we strongly recommend purchasing a power supply with a hardwired voltage transformer rather than a voltage regulator. For power supplies with the same output power, those built with hardwired voltage transformers are usually much heavier than those relying on voltage regulators.

H14. What are the time settings for “Setup” and “Hold”?

A: Setup Time: 0.05ns ~ 0.25ns; Hold Time: 0.02ns ~ 0.08ns.

Clock High requires a minimum of 0.31ns. **Clock Low** requires at least 0.47ns.

6.2 Software

SW01. Why is the compression function not enabled by default?

A: Mostly to avoid significant errors when testing signals with high varieties or measuring a certain channel for a long time period.

SW02. What is the purpose of the compression function?

A: The compression function measures signals that vary slightly over a long period.

SW03. Can I enable Trigger Page and Compression Function simultaneously?

A: Yes, you can.

SW04. When should I use the “Bar” function?

A: This function allows you to highlight a segment of a wave so that you can have a closer view. Depending on the configuration of **Position Display Area Data Mode** under **Tools** → **Customize**, a more accurate numeric value of address, time, or frequency difference will be calculated and displayed as shown in *Fig. 6-1*.

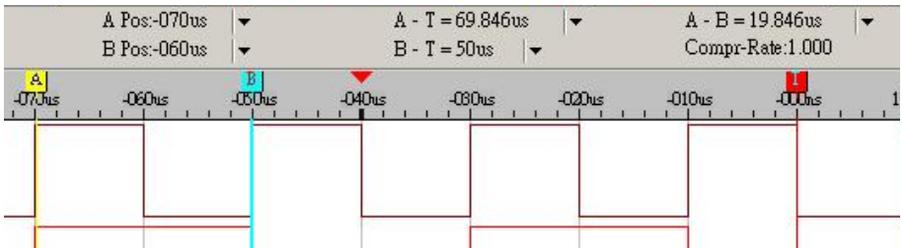


Fig. 6-1 – Bar Function

SW05. Can triggers be differentiated in Pre-Trigger and Post-Trigger?

A: Yes, they can.

SW06. Are all setup parameters and configurations saved as I save my work?

A: No, everything in your work space, except signal graph, will be saved.

SW07. If I have the wheel feature with my mouse (or other pointing devices), may I adjust the wave display zoom, in the Position Display Area, by scrolling?

A: This feature has been enhanced since Ver. 1.03. If your program version is prior to this version, visit our website for the latest update at

http://www.zeroplus.com.tw/new_instrument/main-download.php?type=1

SW08. What are the extremes for Delay Time and Clock & Trigger Delay Clock?

A: The interface will inform you of the interval you may use. However, it varies from case to case, depending on your test devices. See *Fig. 6-2*.

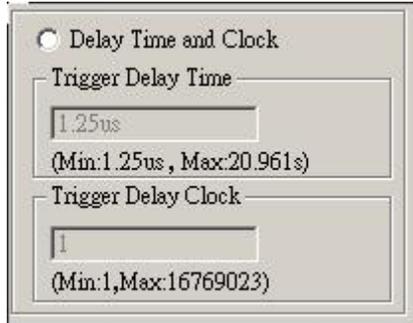


Fig. 6-2 – Delay Time and Clock

SW09. How do I know the version number of my software interface program?

A: Click **Help** from the menu (See *Fig 6-3*), and then select **About the Logic analyzer**(See *Figs 6-3 and 6-4*).

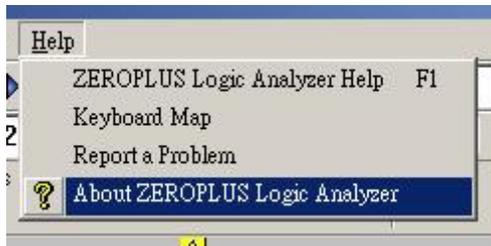


Fig. 6-3 – About Logic Analyzer



Fig. 6-4: The circled information is the version number.

SW10. How may I upgrade my software interface program?

A: Visit our website at <http://www.zeroplus.com.tw> and follow the instructions for the English version. You may also use the following address for English updates.
http://www.zeroplus.com.tw/new_instrument/main-download.php?type=1

SW11. Can I save my signal data to a separate pure text file (*.txt)?

A: This feature will be available in V1.03.01. We apologize for any inconvenience. Visit our website at <http://www.zeroplus.com.tw> for the latest updates.

SW12. Why is the text display covered by other text or outside the display width?

A: At this stage, our software interface program has missing code for multilingual support. You will have to ensure your system default encoding is one of the following languages: 1) any English Encoding (en, en-XX), 2) Traditional Chinese (zh, zh-XX in Big-5), 3) Simplified Chinese (zh, zh-CN in HZ, GB2312, GB18030). Double check the language configuration in **Region and Language Option**.



Fig. 6-5 – Windows Regional and Language Options

SW13. Is there a Reset that restores the default color settings for signal output waves in the Position Signal Display Area?

- A:** Yes, there is. Click **Tools** from the menu, and select **Customize**; click **Restore Defaults**. However, this restores everything in this window. You must make a further adjustment if the color setting is the only thing you want to restore. See Fig. 6-6.

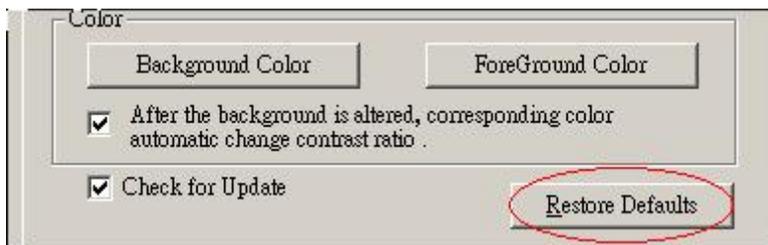


Fig. 6-6 – Restore Color Defaults

SW14. Can I change the wave mode displayed?

- A:** Yes, you can. There are two ways to do this. First, go through **Data → Wave Mode** and choose a waveform. See Fig. 6-7.



Fig. 6-7 – Waveform Shapes

The second alternative is to right-click any place in the Position Display Area. This will pull out a menu. Click **Wave Mode**, and choose a waveform. See Fig. 6-8.

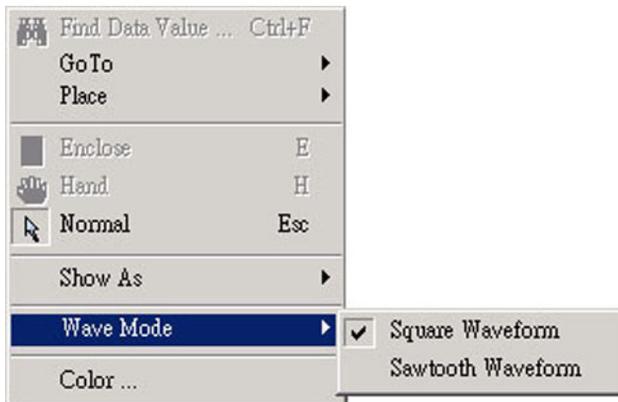


Fig. 6-8 – Wave Mode

SW15. Can I change the Signal Display Mode into the Timing mode?

A: Yes, you can.

SW16. Why does Enable Delay not work when the Double mode is enabled?

A: To optimize signal output quality and maximize memory efficiency, the **Enable** function may work under the Double mode. However, the **Enable Delay** function DOES NOT work under the Double mode, at this stage.

6.3 Registration

RG01. What is the significance of the hardware serial number?

A: Every product is assigned and engraved with a unique serial number, which allows us to trace the original manufacturing date of a specific product.

RG02. How do I register online?

A: Visit our homepage at <http://www.zeroplus.com.tw>. Choose the Instrument Department, and click on **English**. You may also enter the following address: http://www.zeroplus.com.tw/new_instrument/main-member-register.php?flag=insert
Once you finish membership registration, proceed with product registration. After finishing product registration, you will receive an email consisting of your product registration information. A password may be required for further customer services and other inquiries.

RG03. What should I do if online registration fails?

A: Do a screen grab of the window, including the error message, and email our customer service dept. A customer service representative will be glad to assist you as soon as possible, once the email is correctly received.

RG04. How may I register if the purchasing date was longer ago than one calendar month?

A: In this case, fill in the registration card and send it via post , fax , or email to our customer service dept and a representative will process the registration for you.

RG05. What is the warranty length for my product?

A: A two-year FACTORY WARRANTY is offered in which you will have to send the defective product to the closest branch, an authorized service site, or our headquarters. The in-store warranty may vary, and many require extra charges for various extended warranty policies. The company is not be responsible for an in-store warranty that exceeds our factory warranty.

RG06. Why should I register this product?

A: If you do not register this product, the warranty will be counted from the manufacturing date indicated by the serial number of your product. Thus, we strongly recommend registering your product, for your own benefit.

RG07. What should I do if the hardware serial number is previously registered?

A: In this case, take a picture of the decal on the rear side of the product and fill in the registration form. Call us and mail both picture and registration to us. A customer representative will be happy to assist you.

6.4 Technical information

TI01. What is the Logic analyzer?

A: The Logic analyzer is a tool that sieves out and shows the digital signal from test equipment by using a clock pulse. The Logic Analyzers Logic Analyzer is like a digital oscilloscope. However, it only shows two voltage grades (the logic status 1 and 0), differing from the many voltage grades of an oscilloscope. The Logic Analyzers Logic Analyzer has more channels than an oscilloscope to analyze the waveform. Since the Logic Analyzers Logic Analyzer only obtains signals 1 and 0, its sampling frequency is slower than an oscilloscope, which needs many voltage ranks. Moreover, the Logic analyzer can receive many signals during a test.

TI02. How does the Logic Analyzers Logic Analyzer operate?

A: The Logic Analyzers Logic Analyzer reserve trigger requirements sets users and uses them on the test equipment for the value of the sampling signals and puts them into the internal memory. The software of the Logic Analyzers Logic Analyzer will read out the value from the memory and switche it to the waveform or status shown for user analysis.

TI03. What is the asynchronous Timing Mode?

A: Since the sampling clock and tested objects are not directly related to each other, and the former won't be controlled by the latter, the sampling clock and the tested signals will not be done at the same time. We call this "Timing Mode", which means that in the same time interval, you can get sampling data from the test equipment at one time, such as every 10 seconds. The internal clock, the Logic Analyzers Logic Analyzer's inner confirmed one, is often for sampling in Timing Mode as is the logic waveform.

TI04. What is the synchronous State Mode?

A: Because the sampling clock and measured object can be directly related, and are controlled by the latter, signals of the former and the latter can proceed simultaneously. We call this "State Mode". In this mode, the measured object provides the sampling clock. State Mode is when the Logic Analyzers Logic Analyzer can obtain sampling data from the test equipment synchronously. In other words, when the test equipment has a signal or signal group, this is the time to get the signal. For example, while the test equipment is sending out one rising edge, the Logic Analyzers Logic Analyzer can start to obtain one signal.

TI05. What are A-bar, B-bar and T-bar?

A: The T, A and B-bars are labels. T is the trigger label, which cannot be removed when the waveform or the state is displayed, which marks a pod. When searching for, or obtaining data, the A and B labels can be set in any location. Using the order of these markings, you can return quickly to the desired position to analyze data. This can also be a point to measure the interval between A-B, A-T, or B-T.

TI06. What is a Trigger Gripper?

A: A gripper is the gathering point to collect the Logic Analyzers Logic Analyzer channels. When a cable connector is not suitable for the test device, a trigger gripper may be an alternative for connection.

TI07. What is a Channel?

A: The channel is the collection line of the input signal. Each channel is responsible for linking the pin of the measured device. Every channel is used to collect signals from test equipment.

TI08. How can I display acquisition in the waveform captured by external sampling signal?

A: Select **Waveform Display** from the **Window** list.

TI09. What is an External Trigger?

A: An external trigger is a signal outside the Logic Analyzers Logic Analyzer used for the simultaneous test of 2 test tools. For example, one the Logic Analyzers Logic Analyzer can be started by one signal from another test tool. Or when it is triggered, it can output one signal to another test tool. The Logic Analyzers Logic Analyzer is often used for triggering an oscilloscope.

TI10. Why does Double Mode not coincide with Enable Delay?

A: In order to set out the perfect waveform from the Logic Analyzers Logic Analyzer and achieve optimal memory efficiency, you can use the **Enable** when using **Double Mode**; the system doesn't support the function of **Enable Delay**.

TI11. How do I update software?

A: The software will automatically check for and download updates. This function deletes old software first and then downloads & installs the latest version.

6.5 Others

OT01. How was the Logic Analyzers developed?

A: It took us more than two years to develop this product. We envision “Everyone carrying the Logic Analyzers Logic Analyzer,” and we would like to make some contributions to the electronics industry in return. We also wish to transform the stereotypical OEM factory into a world class R&D center.

OT02. Why is there a rich information database for game chips rather than the Logic Analyzers Logic Analyzers?

A: First of all, we apologize for any inconvenience caused by the lack of information pertaining to the Logic Analyzers Logic Analyzers. We are currently working very hard on multilingual information and documentations pertaining to the Logic analyzers. Visit our website for the latest drivers, software, and manuals: http://www.zeroplus.com.tw/new_instrument/index.php?lang=eng. In the meantime, we will have updates ready when verified error free.

OT03. What was the original intention of when developing this item?

A: Originally, the Logic Analyzers Logic Analyzer was just for use by our engineering department. Later on, we saw the greater need for this kind of device. We made numerous enhancements and made it available to the public.

Conclusion

This chapter is full of hard facts for engineers. The contents of this version of the User's Manual may look lot different than the one on the web. Every engineer finds new problems, new solutions, or other issues, during real life applications. Though there are dozens of questions here, we look forward to your feedback, which is important for future versions. It may help us produce more efficient and accurate devices that will offer you much better service.

7 Appendix

7.1 Hot Keys

Objective

In this chapter, users will learn the functions of all defined hot keys in the Logic Analyzer software interface.

7.1 Hot Keys

Table 7-1: Hot Keys (1)

Hot Key	Equivalent Orders	Statement
A	Place the A Bar position	Moves waveform to where the A-bar is centered; select A-Bar by cursor.
B	Place the B Bar position	Moves waveform to where the B-bar is centered; select B-Bar by cursor.
T	Place the T Bar position	Centers T-Bar and cancels other bars.
E	Change to Enclose mode	Changes the mouse mode to Enclose
H	Change to Hand mode	Change the mouse mode to Hand.

Table 7-2: Hot Keys (2)

Hot Key	Equivalent Orders	Statement
Ctrl + A	Place A Bar	Centers A-Bar
Ctrl + B	Place B Bar	Centers B-Bar
Ctrl + C	File -> Graph	Opens Capture Graph dialogue
Ctrl + E	Data ->Enclose	Changes Mouse mode to Enclose mode.
Ctrl + F	Data -> Find Data Value	Searches specific data with predetermined conditions
Ctrl + G	Bus/Signal -> Group into Bus	Groups selected signals into a Bus
Ctrl + N	File -> New	Creates a new file
Ctrl + O	File -> Open	Opens saved file
Ctrl + P	File -> Print	Prints active file
Ctrl + S	File-> Save	Saves active file with its current name, location and file format.
Ctrl + U	Bus/Signal -> Ungroup from Bus	Ungroups signals (Pins) from a Bus.
Ctrl + Z	Data -> Undo last zoom	Reverses last zoom
Ctrl + Shift + E	File->Export	Opens Export Dialog.

Table 7-3: Hot Keys (3)

Hot Key	Equivalent Orders	Statement
Page Down	Operate the position shown	Goes to next page of data or waveform
Page Up	Operate the position shown	Goes to prior page of data or waveform
Home	Operate the position shown	Go to beginning of data or waveform
End	Operate the position shown	Goes to end of data or waveform.
Up	Operate the position shown	Moves cursor up a grid.
Down	Operate the position shown	Moves cursor down a grid.
Left	Operate the position shown	Moves selected Bar or display left to prior waveform or data.
Right	Operate the position shown	Moves selected Bar or display right to posterior waveform or data.
ESC	Operate the position shown	Releases all selected bars, and changes Mouse mode to normal.
Space	Change the trigger conditions	Changes trigger conditions.
Function Keys	Equivalent Orders	Statement

Table 7-4: Hot Keys (4)

Hot Key	Equivalent Orders	Statement
F1	Help -> Logic Analyzer Help	Logic Analyzer Help
F2	Decrease the sampling rate	Decreases sampling rate.
F3	Increase the sampling rate	Increases sampling rate
F5	Run/Stop -> Single Run	Executes acquire once
F6	Run/Stop -> Repetitive Run	Executes acquire continuously
F7	Run/Stop -> Stop	Stops acquiring data
F8	Data -> Zoom out	Zooms out waveform
F9	Data -> Zoom in	Zooms in waveform
F11	Data -> Before	Moves forward to prior variation waveform and centers that location.
F12	Data -> After	Moves forward to next variation waveform and centers that location.

Conclusion

The demonstrations in this user manual will enhance users' understanding of future issues, even though the manual ends here. We thank you for choosing the Logic Analyzer. Please contact us if you feel anything that could be done better, either in software or hardware. We appreciate your input.