Best Measure . Best Quality

ZEROPLUS

Advanced Digital Signal Analyzer

PC-Based Logic Analyzer LAP-A Series

Max

Max RAM Size 512Mbits

Efficiency

Provides I^2C, UART, SPI, 1-WIRE, HDQ, CAN BUS, USB1.1, I^2S etc special bus serial communication Convention Analysis, promotes the working efficiency.

Waveform Compression

High percentage immediate compression signal obtains more data spaces, and captures more analytical data. (TW.Pat.206912)/(UK.Pat.2411482)

Enable Delay

Filters the multifarious and unnecessary signal, achieves the sample analysis optimization. (TW.Pat.I271532)

PC-Based Interface

Windows system and USB2.0 (1.1) high speed transmission; the volume small does not occupy the space, carries conveniently.

Free standard edition software promotion

Two annual products guarantee against damage, consummation post-sale service

Bus Fields of Application

AUTOMOTIVE | DIGITAL AUDIO | MEMORY | PC SYSTEM | IC INTERFACE | OTHER

Analyzing special series digital signal can actually be very relaxed!

Zeroplus Logic Analyzer provides special series communication protocol I²C, UART, SPI, 1-WIRE, HDQ, CAN BUS, USB1.1, displaying in DATA BUS mode and enable delay and page function, which can effectively improve work efficiency. The Logic Analyzer adopts PC-Based interface, the volume is small, and so it does not occupy the space, and carries conveniently; Windows demonstration, simple and easy to use, waveform enlarging, waveform compression, width auto demonstration, file saving and export are conformed to apply. It can correctly and effectively develop, check and complete more special cases that Zeroplus Logic Analyzer integrates with developing you product.

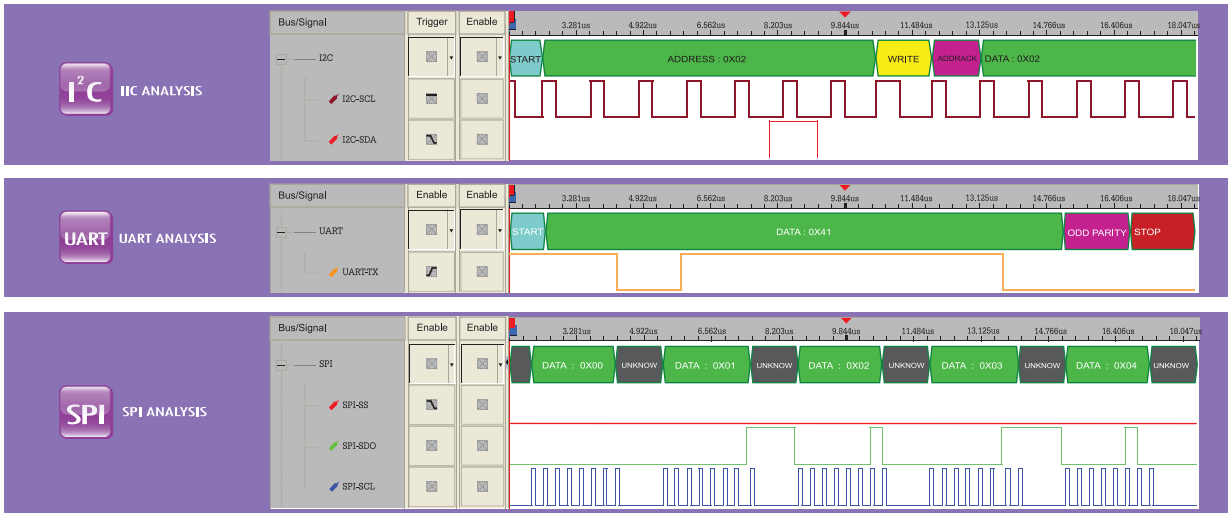
Product Characteristic

Hardware Specification

Sampling Rate 100Hz~200MHz (Timing Mode) and 100 MHz (State Mode)
Test Channel: 16~32CH, Depth (Per Channel): 2K~2MBits

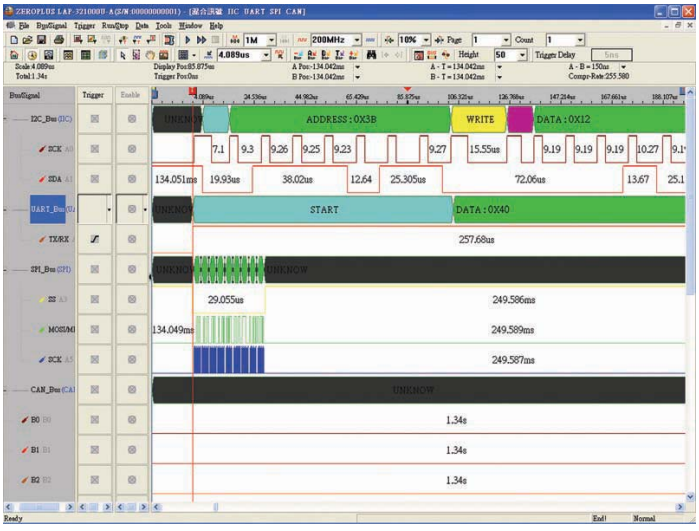
Special Bus Analysis

Starting the special bus analysis function, you may hand over by LA the numerous and diverse data to decode, no longer needs to penetrate the user voluntarily analyze data, which reduces time and error rate, when engineer judges voluntarily the complicated data. Besides the provided I²C, UART, SPI, 1-WIRE, HDQ, CAN BUS, USB1.1 serial signal decoding, we can provide customized serial signal analysis as your requirement, LA can demonstrate the different series signal decoding in the same triggering.



Automatic Demonstration Waveform Width

Automatic Demonstration Waveform Width can easily and fast demonstrates each cycle's time, the frequency and the sampling count, and do not need to use a Cursor section by section to measure slowly again .



Trigger Page

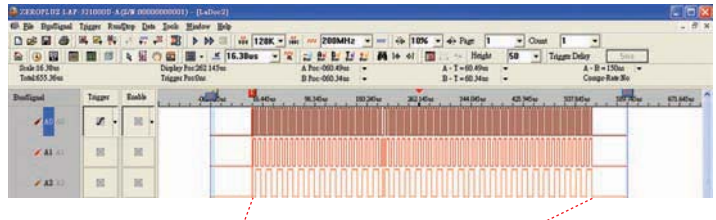
The patent technology of trigger page can inspect in sequence the waveform data by the paging mode, it can separate into at most 128 ~ 8191pages.(TW.Pat.I244266)

Compression

Compression Patent Technology, the memory depth per channel is 128K, after compressing, the compression rate can arrive the highest 255 times, which lets you capture 128K*255=32Mbits sampling data, and the 1M Logic Analyzer can capture 255M bits sampling data. (TW.Pat.206912)/(UK.Pat.2411482)

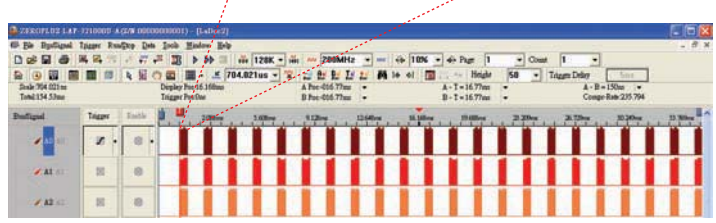
● Uncompressed

Time Total: 655.36us
Compression rate: No



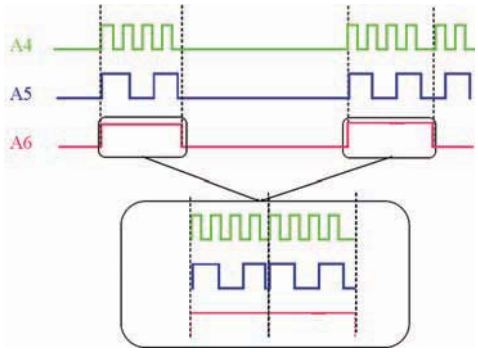
● Compressed

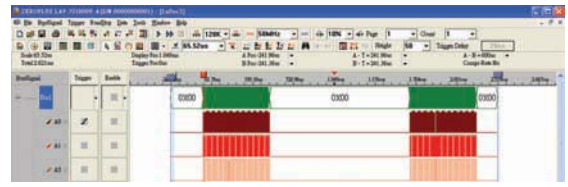
Time Total: 132.364ms
Compression Rate: 201.972

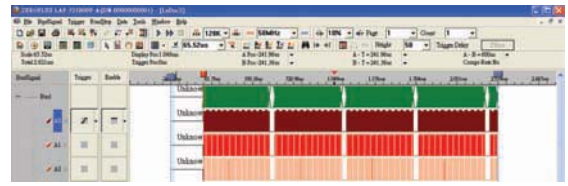


Enable delay

Waveform enable and enable delay technology can filter the unnecessary signal, in order to make use of the memory saving the valuable data and achieve the analysis optimization (TW.Pat.1271532)

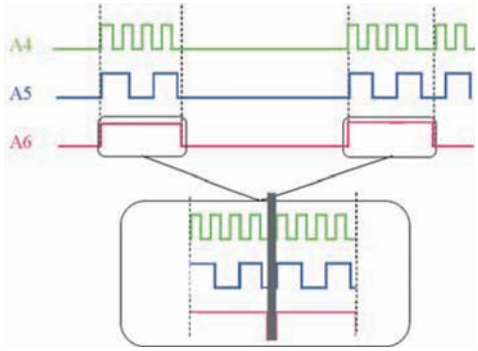


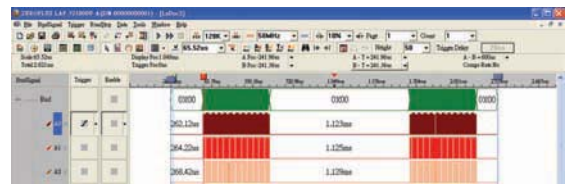


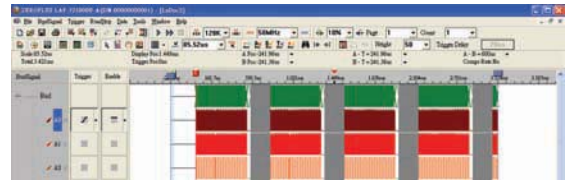


Enable bar

Using Enable bar function makes the memory save the valuable signal, and save the filtered time perfectly. Enable bar can customize its width.







Window Demonstration and User-friendly Operation Interface

Chinese Operating Interface, simple and easy to use. Waveform enlargement inspection, Waveform width demonstrated automatically, Choice analysis data scope, Fast demonstration whole page, Waveform cross-reference demonstration.

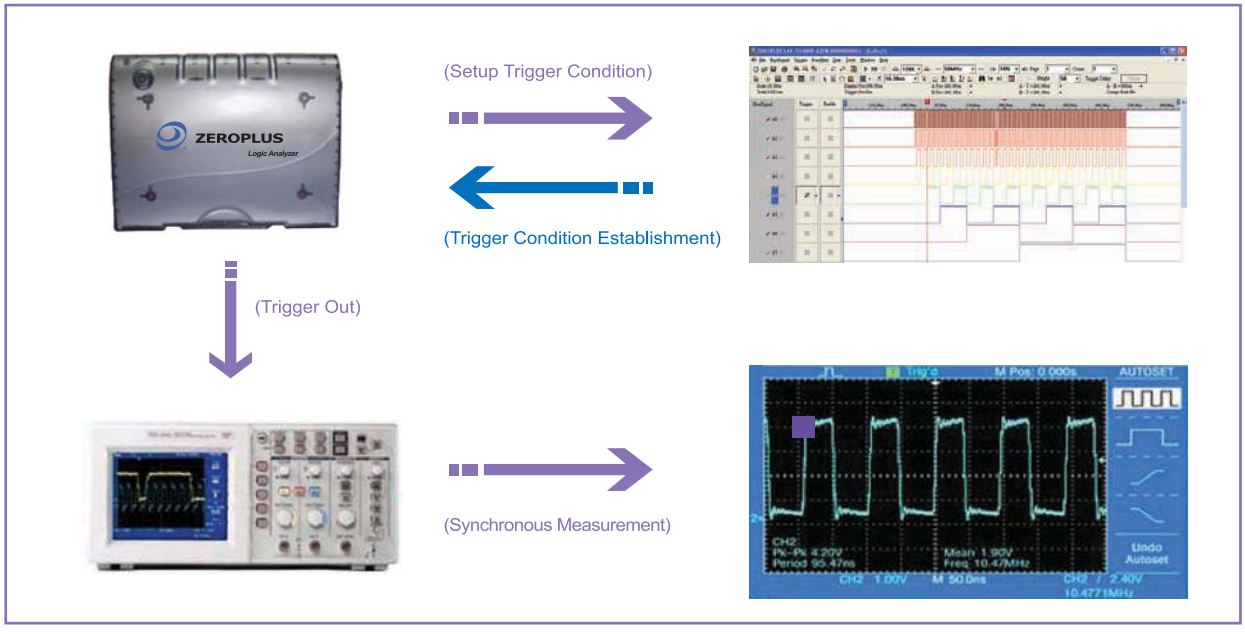
Data Statistic Function and Data Conformity Application

Data Statistic Item:
(1) Full Period
(2) Positive Period
(3) Negative Period
(4) Full Period by Condition
(5) Positive Period Full Period by Condition
(6) Negative Period Full Period by Condition

In addition, it can make file storage, printing and export into common data format.

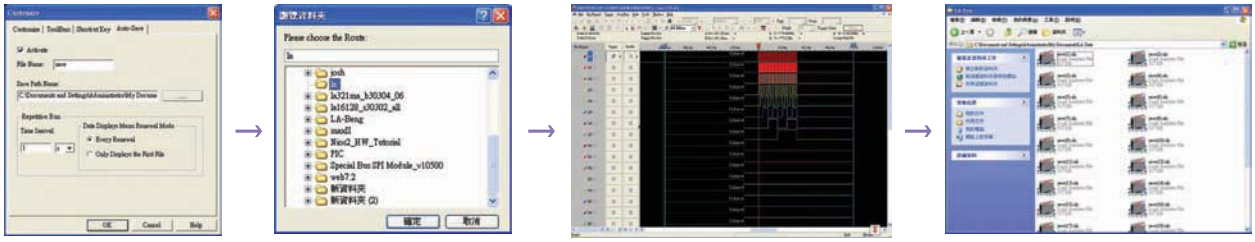
Trigger Out

Trigger Out is, after the setup trigger condition of Logic Analyzer is finished, Logic Analyzer will transfer a signal to another awaiting instrument (Oscillograph / another Logic Analyzer); after the instrument receives the trigger signal, it will do the similar synchronous measure to the device under test. However, The primarily function of logic analyzer primarily is measure data bit signals, and doesn't supply effective analysis for Voltage change and Phase change, so Logic Analyzer has this function, min order to use with Oscillograph matching.



AUTO-SAVE (for long-time monitor record)

This function gives you an easy way to record the digital wave for long-time test now. They need to test a creations is stable or not, when the engineer design a creations. This function will able to help they to record digital wave data in long time. Therefore, they don't need to stay in there.



Standard Fittings

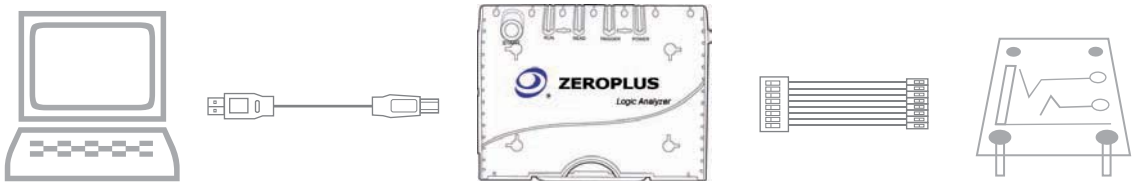
Serial Communication Convention Analysis (Continues to Increase)	LAP-16064U (New)	LAP-16128U	LAP-32128U-A	LAP-321000U-A	LAP-322000U-A (New)
I²C	Free	Free	Free	Free	Free
UART	Free	Free	Free	Free	Free
SPI	Free	Free	Free	Free	Free
1-WIRE	Option	Option	Free	Free	Free
HDQ	Option	Option	Option	Free	Free
CAN BUS	Option	Option	Option	Free	Free
USB 1.1	Option	Option	Option	Option	Option
SIGNIA RF	Option	Option	Option	Option	Option
I²S	Option	Option	Option	Option	Free
PS/2	Option	Option	Option	Option	Free
Microwire	Option	Option	Free	Free	Free
SSI	Option	Option	Free	Free	Free
S/PDIF	Option	Option	Option	Option	Option
Lin Bus	Option	Option	Option	Option	Free
Miller	Option	Option	Free	Free	Free
Manchester	Option	Option	Free	Free	Free
LPC Bus	Option	Option	Option	Option	Option
7-SEGMENT LED	Free	Free	Free	Free	Free

Portable Package

Logic Analyzer	1
Testing hook	16CH(20PCS)/32CH(36PCS)
Testing cables	16CH (8pin*2 / 2pin*1 / 1pin*1) 32CH (16pin*1 / 8pin*2 / 2pin*1 / 1pin*1)
USB Cable	1
Driver CD	1
Getting Started Guide	1
Tool box or portable bag	1

RoHS

LA Use Series Connection Schematic Drawing



Computer — Zeroplus Logic Analyzer — Device Under Test

Product Service

- Supply customized communication convention analysis design service.
- Two annual products guarantee against damage, consummation post-sale service.
- Pass each item of safety certification, the quality has the safeguard.
- Free standard edition software promotion.
- Free enterprise education and training.

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LAP

LAP-16064U/ULAP-16128U/LAP-32128U-A
LAP-321000U-A/LAP-322000U-A

LAP-A Specification

>> NEW

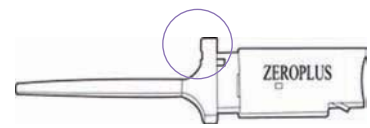
>> 2008.03上市

Product model		LAP-16064U	LAP-16128U	LAP-32128U-A	LAP-321000U-A	LAP-322000U-A
Operating System		Windows 98SE/ME/2000/XP/Vista				
Interface		USB2.0(1.1)				
Sample Rate	Internal Clock (Timing Mode)	100Hz~100MHz	100Hz~200MHz	100Hz~200MHz	100Hz~200MHz	100Hz~200MHz
	External Clock (State Mode)	100MHz	100MHz	100MHz	100MHz	100MHz
Threshold Voltages	Bandwidth	75MHz	75MHz	75MHz	75MHz	75MHz
	Working Range	-6V~+6V	-6V~+6V	-6V~+6V	-6V~+6V	-6V~+6V
	Accuracy	±0.1V	±0.1V	±0.1V	±0.1V	±0.1V
Memory	Memory	2Mbits	4Mbits	4Mbits	32Mbits	64Mbits
	Depth (Per Channel)	64Kbits (Max 16Mbits for Compression)	128Kbits (Max 32Mbits for Compression)	128Kbits (Max 32Mbits for Compression)	1Mbits (Max 255Mbits for Compression)	2Mbits (Max 512Mbits for Compression)
Trigger	Condition	Pattern/Edge	Pattern/Edge	Pattern/Edge	Pattern/Edge	Pattern/Edge
	Trigger Channel	16CH	16CH	32CH	32CH	32CH
	Pre/Post Trigger	YES	YES	YES	YES	YES
	Trigger Level	1 Level	1 Level	1 Level	1 Level	1 Level
	Trigger Count	1~65535	1~65535	1~65535	1~65535	1~65535
Software Functions	Operating Interface Language	Chinese (Simplified)	Chinese (Simplified/Traditional) English	Chinese (Simplified/Traditional) English	Chinese (Simplified/Traditional) English	Chinese (Simplified/Traditional) English
	Time Base Range	5ps~10Ms	5ps~10Ms	5ps~10Ms	5ps~10Ms	5ps~10Ms
	Vertical Sizing	1~5.5	1~5.5	1~5.5	1~5.5	1~5.5
	Enable Delay	YES	YES	YES	YES	YES
	Data Compression	Max. 16Mbits	Max. 32Mbits	Max. 32Mbits	Max. 255Mbits	Max. 512Mbits
	Width Display	YES	YES	YES	YES	YES
	Max Trigger Page	128~8192 Pages	128~8192 Pages	128~8192 Pages	16~8192 Pages	16~8192 Pages
	Trigger Delay	YES	YES	YES	YES	YES
	Infinite Increase Spacer Bar	YES	YES	YES	YES	YES
	Automatic Zoom In of Spacer Bar	YES	YES	YES	YES	YES
	Automatic Software Upgrade	YES	YES	YES	YES	YES
	Data Range Selectable	YES	YES	YES	YES	YES
	Statistic	YES	YES	YES	YES	YES
	Bus Inquiry and Counter	YES	YES	YES	YES	YES
	Enable Bar	YES	YES	YES	YES	YES
	Bus Analyzer Module Plug-In	YES	YES	YES	YES	YES
	Bus package list	YES	YES	YES	YES	YES
Phase Errors		<1.5ns				
Power	Power	USB				
	Power at rest	1W				
	Power at work	2W				
Maximum Input Voltage		±30V				
Impedance		500KΩ/10pF				
Safety Certification		FCC / CE / WEEE / RoHS				
Product Dimension		130mm*100mm*30mm				

Logic Analyzer

Left Side View

Broaden, Skid Resistant Special Design



Special Design Probe

ZEROPLUS

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